Printed Circuit Board Design can Impact Electrochemical Reliability

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Abstract
Highly dense printed circuit board assemblies (PCBAs) build in more functionality using leadless components. Over the past several years, bottom terminated components (BTCs) have continued to gain popularity and usage for their signal integrity, thermal, and power dissipation properties. While these packages offer gains in electrical functionality, they also pose challenges to ensure high quality and high-reliability operation. Thermal pads, thermal vias, and spacings between power/ground domains present unique challenges for the package type. One of those challenges is the risk of dendritic growth, leading to power-to-ground shorting or unwanted leakage currents. The condition may occur if unactivated flux residues remain between a BTC device and the printed circuit board after soldering.

The study examines IPC 7093A Printed Board Design Considerations for Bottom Terminated Components. New BTC guidelines are being issued by IPC outlining critical design and process elements needed to assemble BTCs onto printed circuit board assemblies. A test vehicle was designed to examine SIR performance of two crucial BTC design points (a) open copper and (b) SMD thermal pads – spanning the range of IPC 7093 thermal pad options.

Decisions made during the bare board design phase can have a direct impact on the activity of the flux residue located under the bottom termination. The purpose of this study focuses on the design elements that improve flux outgassing. Past research finds that proper outgassing improves electrochemical reliability, especially when the device is exposed to atmospheric moisture.

Key Words: Bottom Terminated Components, BTCs, QFN, BTC Electrochemical Reliability

Introduction

Bottom Terminated Components (BTCs) are leadless components with terminations located on the underside of the component. These high-performance packages are attractive to designers due to their low cost and functional performance. BTCs incorporate solderable terminations that are flush with the bottom of the package. They can also have smaller solderable termination areas located along the perimeter sides or flanks of the package near the bottom of the device.

Consumer electronics drive BTC electronic packaging technologies. Size reduction and increased functionality are key drivers[1]. The BTC component family meets these requirements with higher performance, reduced power consumption, size, and off the shelf availability. The low profile BTC finds an application on highly compact designs where weight and package thickness are minimized.

The body outline dimensions range from 1 mm^2 or as large as 12 mm^2. Contact pitch is commonly less than 1 mm and a die element that is nearly the same size as the package (Figure 1). The lack of traditional leads or balls allows for reduced package thickness. The narrow pitch and thin package create a low gap from the surface of the board to the bottom of the package (Figure 2). Low standoff gaps can block flux outgassing channels during the reflow process. When this occurs, flux residues build upon themselves. The amount of residue trapped under the bottom termination increases. The residue can be pliable since some of the carrier solvent, activator, and functional additives are not properly outgassed and decomposed.

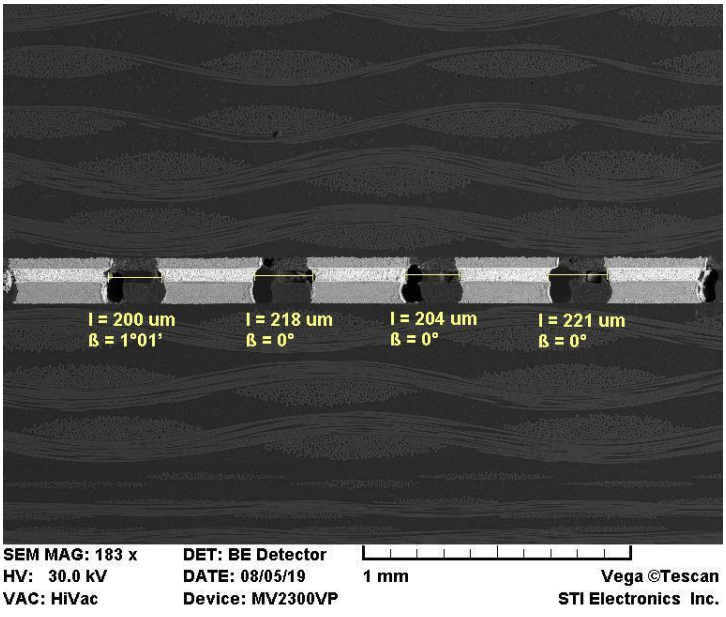

Figure 1: Contact Pitch of the I/O Lands

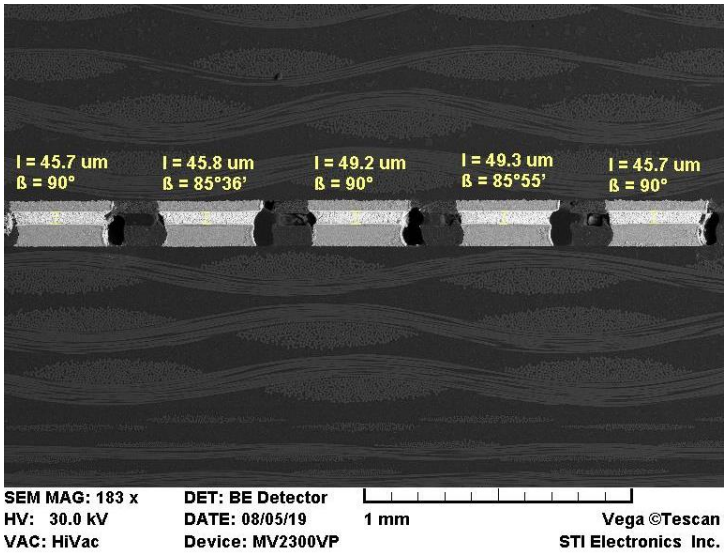

Figure 2: Narrow Pitch and Low Standoff Gap

Problem Statement

The use of no-clean flux systems is designed to leave a benign surface residue following the reflow soldering process. The problem is that the low standoff height in combination with the variation of temperatures at the bottom termination during soldering can result in pockets of active localized ionic residues under the bottom termination[4].

Flux residues and other ionic contaminants left under the BTCs can bridge the I/O signal pins and between the I/O and thermal pad during the assembly process. If atmospheric moisture is present, these residues are a potential threat to current leakage and corrosion. No-Clean flux systems should, in principle, only leave benign surface contaminants. However, results show that the variation in reflow temperature at the devices bottom termination and standoff gap can result in considerable amounts of localized residues[4].

The flux activator and solvent carrier are designed to decompose at specific temperature ranges[5]. Low standoff gaps can both shield and prevent some of the solvent carrier and activator from properly decomposing. This condition results in more residues left under the bottom termination following the reflow process. The blocked outgassing and reflow temperature effects can result in the lack of a suitable rosin/resin oxygen barrier to encapsulate problematic residues and to forming a truly benign surface residue.

When the BTC on the finished product is exposed to humid conditions, components of the flux residues (especially the carboxylic acid content) in contact with mono-layers of water can cause intermittent failures[4]. Leakage currents between biased points on the BTC reduce surface insulation resistance (SIR). Weak organic acid residues are hygroscopic and therefore influence the amount of water adsorption under humid conditions. Subsequent dissolution of the active part of the flux into the adsorbed water layer then influences the SIR followed by detrimental electrochemical processes at biased metallic connections. These mechanisms have a direct impact on the reliability and lifetime of electronics.

Purpose of the Research

BTC component designs differ across suppliers. The non-standard design varies the component pitch, pad dimension, pad size, and shape[3]. The solder interconnect is formed solely by solder paste applied at the bottom assembly. Small solder connections result in a low standoff height of approximately that can range from 1-3 mils. This low standoff can block flux outgassing channels during the soldering process. The level and activity of the soldering residues may be impacted by these conditions.

The solder paste is the vehicle that provides the flux and solder alloy necessary for a reliable and consistent assembly process. A low residue, no-clean solder paste is commonly used. Solder paste is composed of the alloy in combination with a rosin/resin vehicle, solvent carrier, heat stabilizers, activators, thickeners, rheological agents, and surfactants. This complex blend and the conditions used to reflow the BTC are critical to forming reliable solder connections.

To minimize voids, dissipate heat, and improve flux outgassing, plated thermal vias can be placed within the thermal lug. Thermal vias provide channels for heat dissipation. Thermal vias also reduce voiding within the thermal lug. Another potential benefit is a channel for flux outgassing (Figure 3). The purpose of this research is to evaluate the plated via diameter hole size as an outgassing channel for the flux vehicle. The surface insulation resistance at the I/O signal pins and the I/O to thermal lug will be measured. Higher surface insulation resistance values indicate that the flux residue has been appropriately outgassed and catalyzed.

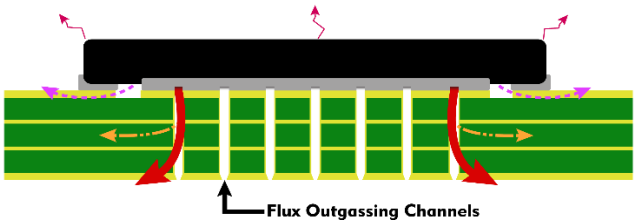

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Figure 3: Plated vias into the thermal lug region

Test Vehicle

A test vehicle was designed to examine SIR performance of flux residue trapped under the bottom termination. The test vehicle has four quadrants with (a) open copper in two quadrants and (b) SMD thermal pads in two quadrants (Figure 4). Solder mask definition of the I/O signal pins used both the singulated and ganged design. The outgassing channels consisted of five thermal vias placed at the corners and in the center of the thermal lug under the QFN component. Each quadrant was designed to compare different board design features and the effects these features provide in flux outgassing.

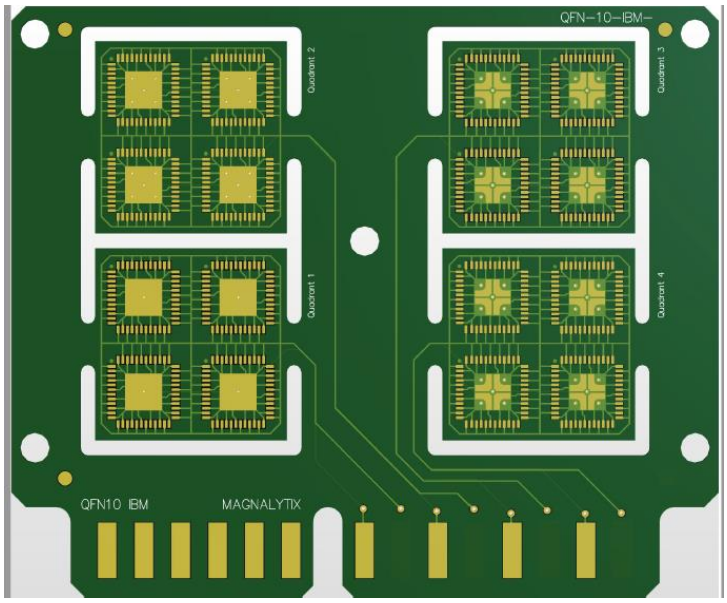

Figure 4: Test Vehicle Designed to Examine SIR Performance

Quadrant Test Parameters

- Quadrant 1
  - Open Copper
  - Singulated I/O
  - 8 mil thermal vias placed into the thermal pad
- Quadrant 2
  - Open Copper
  - Ganged I/O
  - 8 mil thermal vias placed into the thermal pad
- Quadrant 3
  - SMD Thermal Pads
  - Ganged I/O
  - Encroached Vias
  - 8 mil thermal vias within a solder mask web
- Quadrant 4
  - SMD Thermal Pads
  - Singulated I/O
  - Encroached Vias
  - 8 mil thermal vias within a solder mask web

The design features across the four quadrants include the following:

1. Solder Mask Design for I/O ENIG signal pins - Both the Singulated and Ganged solder mask defined I/O pads were used on the test board (Figure 4).

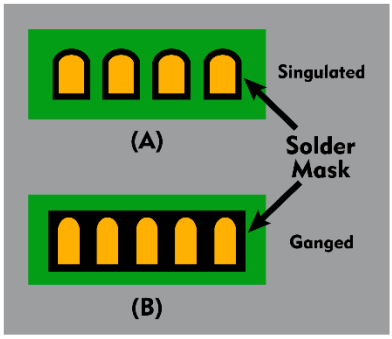

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Figure 4: Singulated (A) compared to Ganged (B)

Solder mask is a thin polymer layer that is applied to cover the Cu traces on a printed board for protection against oxidation and to prevent solder bridging between closely spaced singnal pins[6]. Singulated I/O pads pattern solder resist apertures that are larger than the metal land geometry. The use of the singulated design for I/O signal pins is generally preferred because it ensures properly formed solder joints between the component lead and the PCB copper pad.

The ganged design removes solder mask across the I/O signal pins. One possible benefit of the ganged design is the increased area for flux to outgas during reflow. A negative tradeoff of the ganged solder mask design is the increased potential of I/O pad solder bridging.

2. Open Copper with thermal vias – thermal vias provide a pathway for thermal heat dissipation, reduce voiding and create an avenue for flux outgassing. The limitation of the open copper design is the potential for the solder to flow through the via to the backside of the board. When this occurs, a bump on the backside of the board is formed, which is not desirable.
3. Encroached vias - Encroached vias within a solder mask web shields solder from contacting the encroached via, thus preventing solder from filling the plated through-hole. Encroached vias take the primary solder mask opening and adjust it so it is slightly larger than the via hole size (typically 50 µm to 200 µm). Encroached vias provide a pathway for both thermal heat dissipation and flux outgassing.

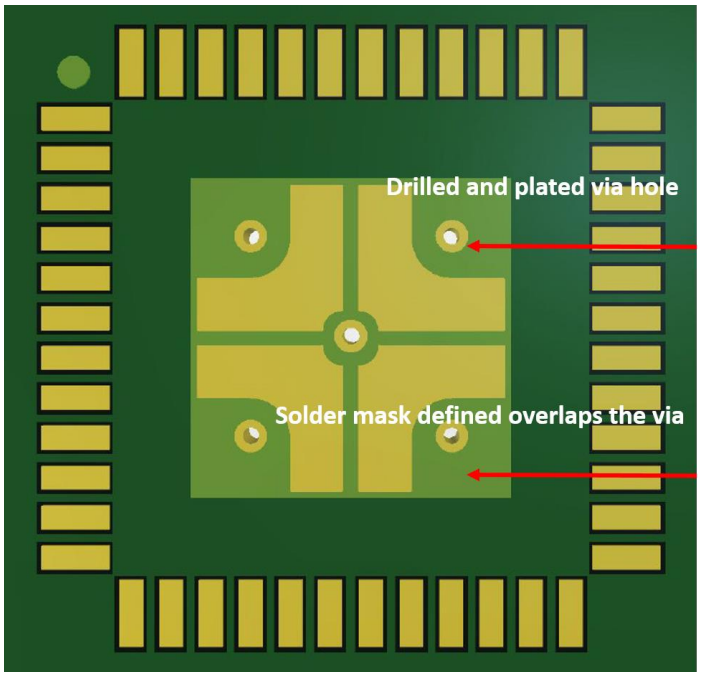

Figure 5: Encroached Via within a Solder Mask Web

Experimental

Eight SIR test boards were populated with 48 pin QFN components. There were four QFN's daisy-chained within each quadrant. A high-reliability SAC 305 No-Clean solder paste using the Ramp-To-Spike Reflow profile was used for assembling the components onto the test board.

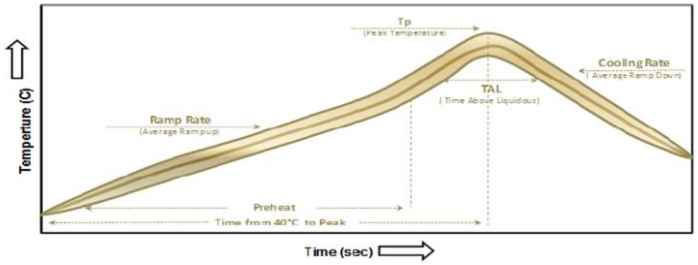

Figure 6: Ramp to Spike Reflow Profile

Before the assembly of the test boards, the boards were pre-cleaned. A blank test board was tested for ionic cleanliness using Ion Chromatography. The baseline cleanliness of the test boards is shown in Table 1.

Table 1: Bare Board Cleanliness

Anion Data (µg/in^2)	
Fluoride	N/D
Chloride	0.21
Nitrite	N/D
Sulfate	0.14
Bromide	N/D
Nitrate	0.24
Phosphate	N/D
Total Weak Organic Acids	6.74
Cation Data (µg/in^2)	
Lithium	N/D
Sodium	0.57
Ammonium	0.82
Potassium	0.24
Magnesium	0.10
Calcium	0.43

Following assembly, the test boards underwent temperature-humidity-bias testing using surface insulation resistance. The method followed was IPC TM-650 2.6.3.7.

Data Findings

Before starting the SIR test, a system validation was run to assure that the high impedance meter readings were within calibration. Each of the channels tested passed validation.

- 1 – Giga-Ohm Through Hole Resistor
- 1 – 100 Mega-Ohm Through Hole Resistor
- 1 – 10 Mega-Ohm Through Hole Resistor
- 1 – 1 Mega-Ohm Through Hole Resistor

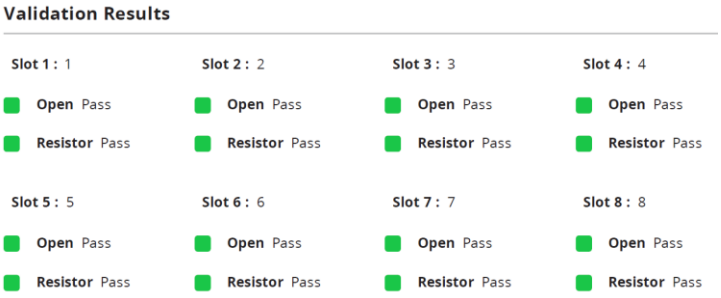

Figure 7: System Validation

The chamber environmentals were consistent over the test period.

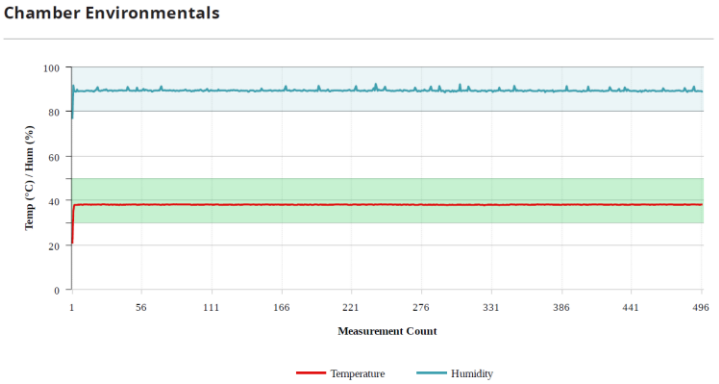

Figure 8: Environmental Conditions during the Test Period

Across the eight test boards, an average of the SIR values are shown in Figure 9. Channel A (Singualted Signal Pins in Open Copper with

No Vias) and Channel D (Singulated Signal Pins in with Solder Mask Defined Thermal Pads) exhibited the highest SIR values. The high SIR values indicate the potential for a robust design.

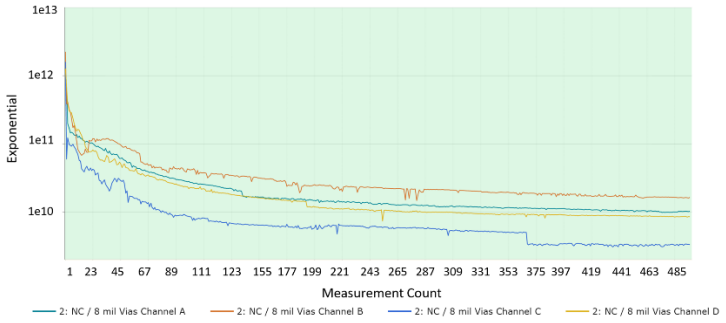

Figure 8: Average of SIR values across the 8 boards tested

Even though the SIR values in Figure 8 are good, there was variability across the eight boards tested. For example, the SIR values for Board 1 (Figure 9) were very consistent. The SIR values for Board 2 (Figure 10) find ionic movement early in the test but stabilized out over the test period. The SIR values for Board 8 (Figure 11) were inconsistent.

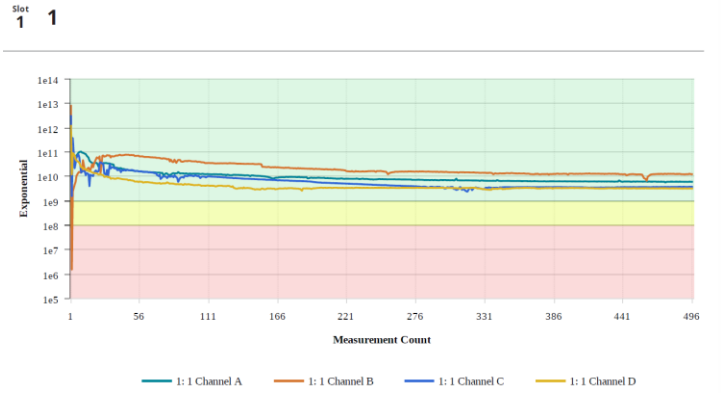

Figure 9: SIR values for Board 1

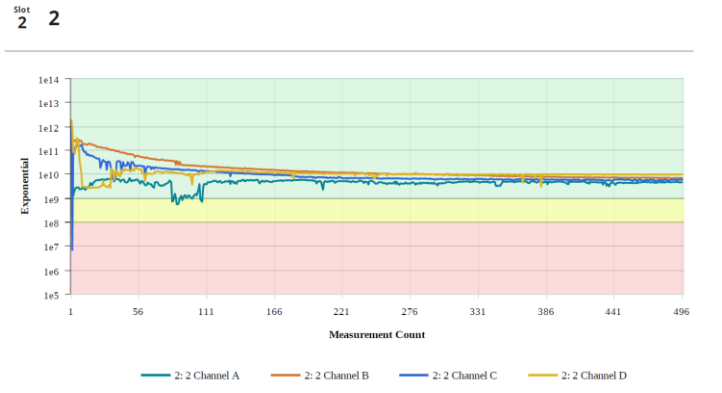

Figure 10: SIR valiues for Board 2

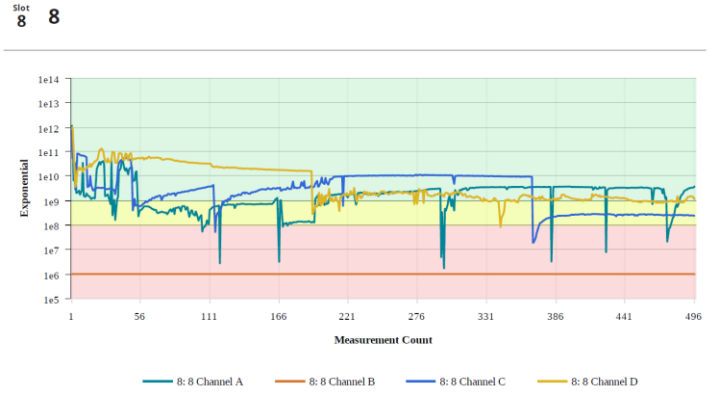

Figure 11: SIR values for Board 9

The research team investigated the variability across the eight test boards. Inconsistencies in the via size were found. Additionally, the copper plating through the via tended to pool near the center of the plated via, which narrowed the pathway through the via.

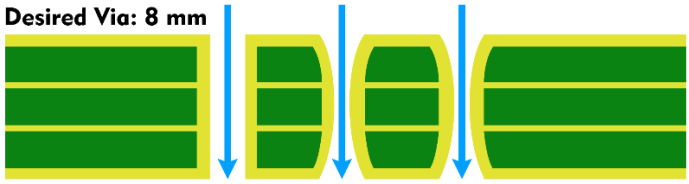

Figure 12: Inconsistency in 8 mil vias

Components were removed from boards that showed ionic movement within the channels. Figure 13 shows some evidence of corrosion at the encroached via.

Figure 13: Corrosion path at the encroached via

The research team ran an additional set of tests to further explore the via size and outgassing channel. Four of the test boards with 8 mil vias were precision drilled the vias to 12 mils (Figure 14). These four test boards were assembled with the QFN's, and SIR tested.

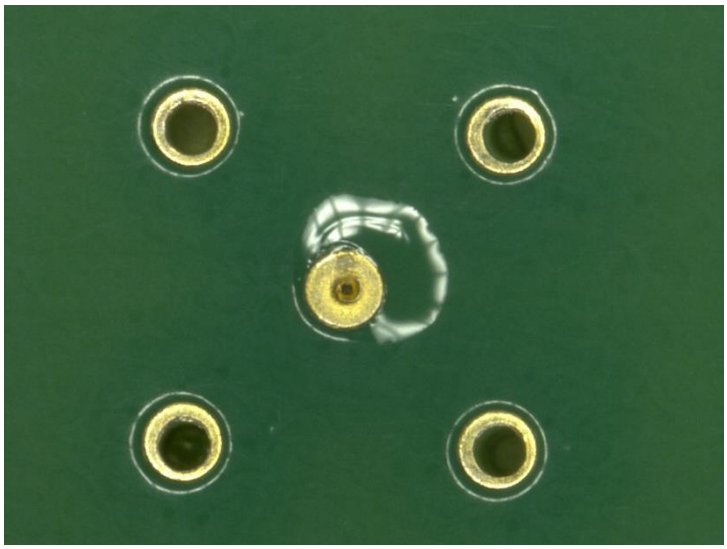

Figure 14: 8 mil vias drilled out to 12 mil vias

The boards tested with the larger via size also had good SIR values. Each of the channels was consistent over the SIR test period. Channel B & C, the ganged design was slightly better than Channel D, the singulated design with solder mask defined vias.

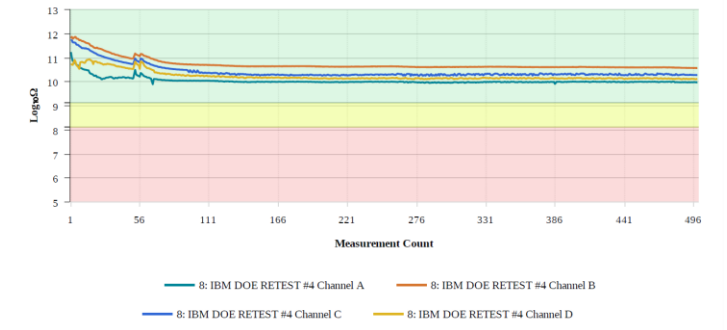

Figure 15: SIR data from the 12 mil via design

Inferences from the Data Findings

Bottom terminated components exhibit a small footprint, tight pitch between signal pins and large thermal lug. The low standoff gap can block flux outgassing channels. These blocked channels increase the level of flux located under the bottom termination. When the solvent and activator portions of the flux residue are not properly outgassed and decomposed, the flux residue can be pliable and ionic. In the presence of atmospheric moisture and bias, the ionic residue under the component can form leakage currents and dendritic growth. These effects can cause intermittent and device failure.

IPC 7093A provides guidelines to assemblers of BTC components. Solder Mask Defined vias are considered best practice for thermal dissipation and reduced voiding. These via structures can also be beneficial for outgassing the flux component of the solder paste during the reflow step.

The research data finds evidence that outgassing vias can also be beneficial to leave a benign flux residue that is less problematic in the presence of atmospheric moisture and temperature.

The optimal via size and placement still needs better definition. The SIR test method with specifically designed test boards is an effective method for optimizing the printed circuit board design. Additionally, the SIR method is effective at characterizing solder materials, reflow profiles, and cleaning methods.

Follow-on Research

Additional work is needed to better understand the design features that impact flux outgassing. Printed circuit board designs that follow the IPC 7093A guidelines provide the right direction to determine best practice. More work is planned using custom test boards that can be tested using the SIR test method.

Acknowledgements

Research is strengthened through collaborative efforts. Subject matter experts in various fields allow researchers to leverage past experiences. The authors thank Matt Kelly and Mark Jeanson from IBM for guidance in the design rules documented in IPC 7093.

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