Risk Management of Class 3 Electronics as a Function of Cleanliness

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Abstract:
In the design and development of safe, effect devices, reducing risk, and ensuring reliability are a manufacturer's first responsibility. The advanced technology inherent in Class 3 hardware and their production means that all aspects of the system – including mechanics, electronics, software, and hardware must be evaluated for reliability. Every aspect of its development – from design and prototyping through manufacture, distribution, disposal, and decommissioning must adhere to strict quality standards that are documented and traceable to functional and safety requirements.

Risk management involves the systematic application of policies, procedures, and practices to the task of analyzing, evaluating, controlling, and monitoring the risk inherent in Class 3 hardware. Risk management is an iterative process that should assess all aspects of the product's lifecycle and must be implemented and documented throughout the design, development, prototyping, manufacture, and phases of a product's lifecycle to ensure that no new or unexpectedly severe risks go unmanaged.

Electronic assemblies are prone to intermittent and total failure from process contamination. Testing is needed to qualify solder materials, reflow conditions, and cleaning processes. Contamination trapped under leadless components is highly problematic due to the pitch reduction, shadowing effects of high components next to bottom terminated components, actively of residues, voltage bias, and environmental exposure. The purpose of this research paper is to apply risk management to contamination. The designed experiments are focused on improved methods for proving out and developing better methods at the point of the manufacturing process for qualifying soldering and cleaning processes that result in acceptable levels of flux and other residues.

Introduction

Reliability is the ability of a product to properly function, within specific performance limits, for a specific period of time, under the life cycle application conditions[1]. Specific performance limits require the product to function within certain tolerances in order to be reliable. Specific period of time means that the product has a useful life during which it is expected to function within specifications. Under life cycle application conditions means that the product is reliable within its operational and environmental conditions.

Generally, contamination failures do not just happen. Failures arise from conditions applied during assembly and any of the following stages of a product's life cycle:

- Product design
  - Bare Board
  - Components
  - Layout
- Assembly
  - Materials selection
  - Handling
  - Stencil Printing
  - Pick and Placing Components
  - Reflow conditions
  - Soldering steps throughout the board build process
  - Cleaning conditions
  - Conformal coating
- Storage
- Packaging
- Transportation
- The products end-use environment

The issue is that the damage or failure mode may not be detected until the later phases of the life cycle.

When a failure occurs, root cause analysis has four major objectives:

1. Verify that a failure occurred
2. Determine the symptom or the apparent way a part has failed (the mode)
3. Determine the mechanism and the root cause of the failure
4. Recommend corrective and preventive action

Before performing a root cause analysis, researchers evaluate all possible symptoms to the root causes of failure. Symptoms are manifestations of a problem that indicates a failure exists. An example is performing a SIR test where the surface insulation resistance values are trending below 100 megohms (1e 8^{th} Log Ohms). An apparent cause is a superficial reason for the failure. An example is the ionic residues that remain near the conductive pathways at the surface or under the components bottom termination. The root cause is the most basic causal factor. For example, a component has a low standoff gap that prevents flux outgassing. As a result, the flux located under the component termination is active. The low standoff gap may prevent the cleaning fluid from penetrating, wetting, and removing errant flux residues.

Root cause analysis is designed to determine:

1. WHAT happened during a particular occurrence
2. HOW it happened
3. Understand WHY it happened

Only when one can determine WHY an event or failure occurred, will one be able to determine corrective measures. Over time, the root causes identified can be used to target major opportunities for improvement.

When considering opportunities for improvement, researchers commonly evaluate failure modes and the effects to identify all possible failures in the design, the manufacturing or assembly process, or a product or service. Knowledge of stress points combined with failure models allows the research team to prioritize failure mechanisms according to their severity and likelihood of occurrence. The FMEA methodology requires:

1. Identify a failure mode
2. Identify the likely cause of failure
3. Identify the failures probability of occurrence
4. Establish the likelihood of detection
5. Identify and prove out corrective actions

Purpose of the Research

Electronic components have continued to reduce in size. Component miniaturization narrows the pitch between conductors. The pathway for contamination to migrate electrochemically from the anode to the cathode increases. As a result, the cleanliness of these electronic components is critical to reliability. The research team is interested in understanding and controlling failure due to contamination.

The purpose of this research is to prove out the SIR test method on test vehicles populated with critical components that are used on production hardware. The test method is designed to track contamination-related failures using highly accelerated test conditions. The test methodology allows for a systematic and detailed assessment of temperature – humidity – bias testing at specific points on selected component lands and under the bottom termination. The test methodologies allow the research team to perform root-cause failure mechanisms on the chosen components representative of the potential failure sites.

The research team plans to use data analysis to perform a FEMA analysis. The goal is to identify the failure mode, the likely cause of failure, the probability of occurrence, the likelihood to detect these causes at the production site, and to identify and prove out corrective actions.

Problem Statement

Highly dense electronics use leadless component bodies that are increasing to miniaturize. Residues trapped under the bottom termination and next to the lands can cause both intermittent and total failure. The problem is threefold. First, low standoff gaps block flux outgassing channels. Solvents and activators formulated in the flux package are designed to decompose as specific points during the temperature rise during reflow. The mass of solder under many leadless components in combination with a low standoff gap can shield the flux from reaching its designed outgassing temperatures. Under these conditions, the amount and the softness of the flux residue increases.

Second, the distance between conductors is so close that the span for metal oxides to migrate is less. Coulomb's law is an experimental law of physics that quantifies the amount of force between two stationary, electrically charged particles[2]. As the distance between conductors narrow, the electrostatic force of oppositely charged particles increases. Metal oxides are removed from the metal surface during the soldering process. These metal ions are encapsulated into the flux residue. When flux residue is both pliable and active, the potential to react with the metal oxide increases. Leakage currents, which slow response time and dendritic shorts between the cathode and anode, can impact device reliability.

Third, electronics are no longer in controlled environments. Climatic reliability must be considered. Flux residues and other ionic residues left on a printed circuit board assembly are a potential threat from moisture that can form on the PCB due to atmospheric conditions[3]. The current use of no-clean flux systems should, in principle, only leave benign surface contaminants. The variation in temperature on the PCB surface during soldering due to thermal and process conditions can result in considerable amounts of localized residues[3].

Experimental

Residues trapped under bottom terminations are not readily visible, even when imaging the side of a component. The cleaning tools and cleaning materials do an effective job of removing flux residues. Surface residues are not a problem to clean. Residues trapped under leadless components require flow channels that penetrate, wet, dissolve and flush these residues away.

Traditional process control methods are not effective in quantitating the activity and risk factors of residues located under the body of a component. Some components are more problematic to contaminated failures than others. To address this problem, there is a need for quantifiable data to identify these site-specific residues and to determine if these residues create an electrochemical migration risk.

SIR testing measures the changes in the surface insulation resistance of a pre-selected material set on a representative test coupon. SIR is the preferred method for quantifying harmful effects that might arise from solder flux or other process residues left on external surfaces after soldering, which can cause unwanted electrochemical reactions that grossly affect reliability[4]. SIR measurements are taken at specific time intervals over the life of the test.

The assembly process involves several different process materials including solder flux, solder paste, solder wire, underfill materials, adhesives, staking compounds, temporary masking materials, cleaning solvents, conformal coatings and more. The test used for this research employs a test condition of 40^0C and 90% relative humidity. The voltage bias applied to the test patterns was 5 volts.

Testing is a 'site-specific' qualification process that should be performed on hardware built at the manufacturer's location. The board is designed into quadrants, with each quadrant populated with different component types. Sensors are routed to the bottom termination where the flux residue is trapped. The component specifications and test are documented and illustrated below.

Test Board used for this study is illustrated below:

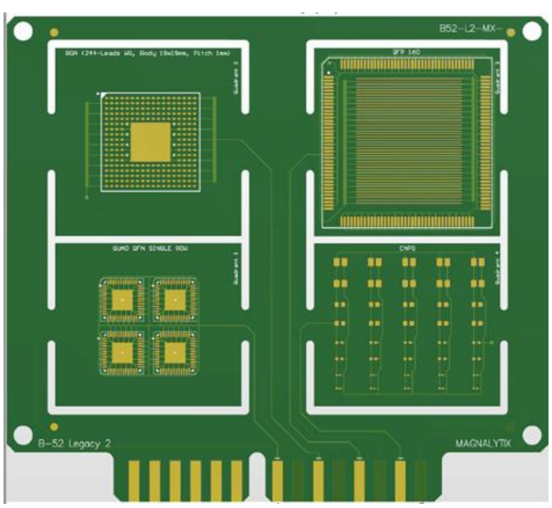

Figure 1: SIR Test Board

Quadrant 1

- QFN 48-T
  - 48 Leads
  - 7x7 mm
  - 0.5 mm Pitch
- Cleaning Challenge
  - Standoff ~ 25-40µm
  - Large solder mass
  - Flux residue may not properly outgas
  - Errant residue can cause electrochemical migration

Quadrant 2

- FBGA
  - 244 I/O
  - 7x7mm
  - 0.5 mm Pitch
- Cleaning Challenge
  - Standoff ~ 25-100µm
  - Large standoff improves cleanability
  - When standoff is below 30µm, the residue next to the center lug can be challenging to clean and lower SIR resistance

Quadrant 3

- QFP 160
  - 160 Leads
  - 28x28 mm
  - 0.65 mm Pitch
- Cleaning Challenge
  - Standoff ~ 100-150µm
  - Tight pitch can trap wash fluids. The SIR comb pattern detects rinse effectiveness
  - Tight pitch can restrict flow channels

Quadrant 4

- Caps
  - 0805
  - 0603
  - 0402
  - 0201
- Cleaning Challenge
  - Standoff ~ 8-30µm
  - Flux residue bridges conductors
  - Difficult to penetrate and remove all residues

Three soldering materials were selected for this study:

1. High reliability No-Clean solder paste
2. Jet printed No-Clean solder paste
3. Water soluble solder paste

Two cleaning processes were studied:

1. Inline Cleaning Machine
    a. 16 minute wash exposure
    b. Fan/Coherent jets
    c. 155°F wash temperature
    d. 18% Wash Fluid
    e. DI Water Rinse
2. Cabinet Style Batch Cleaning Machine
    a. 15 minute wash exposure
    b. 140° wash temperature
    c. 15% Wash Fluid
    d. DI Water Rinse to 250Ω

Responses:

- SIR – IPC Method 2.6.3.7
    - 40°C/90%RH/5V
- X-Ray
- Ion Chromatography
    - Separate IC for each quadrant
    - Inline cleaned boards
    - Batch cleaned boards
    - No-Clean and Water Soluble Solder Pastes
- Visual – Side View
- Standoff Gap

For each condition, there was 3 replicates.

The aggregate of those findings will be reported in Main Effect Plots.

Data Findings

1. No-Clean Solder Paste
    a. Not Cleaned
    b. Inline Cleaned
    c. Batch Cleaned

No-Clean Solder Paste

Not Cleaned:

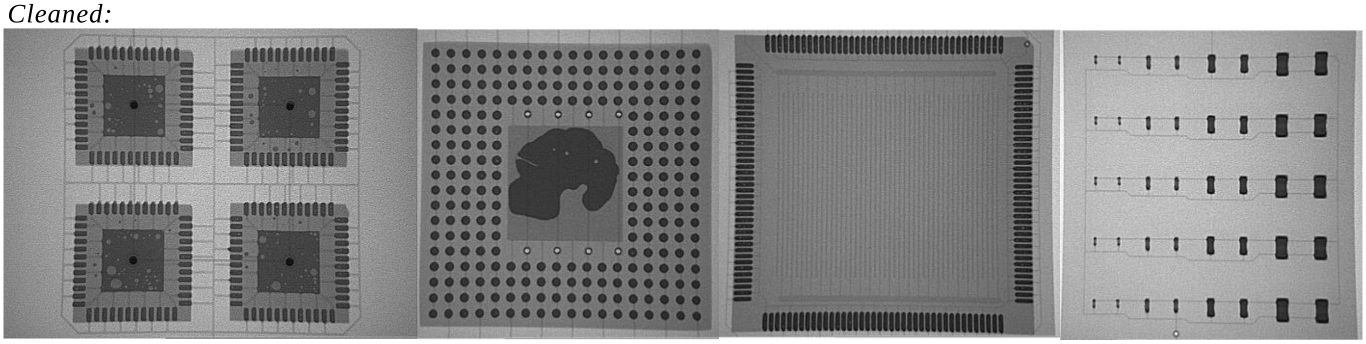

Figure 2: X-Ray Images of the No-Clean Solder Paste that was not cleaned

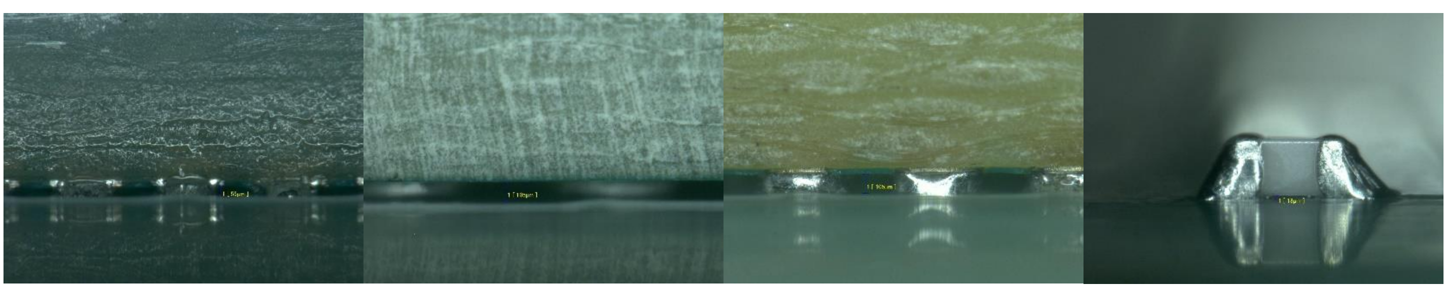

Figure 3: Side Views of the No-Clean Solder Paste that was not cleaned

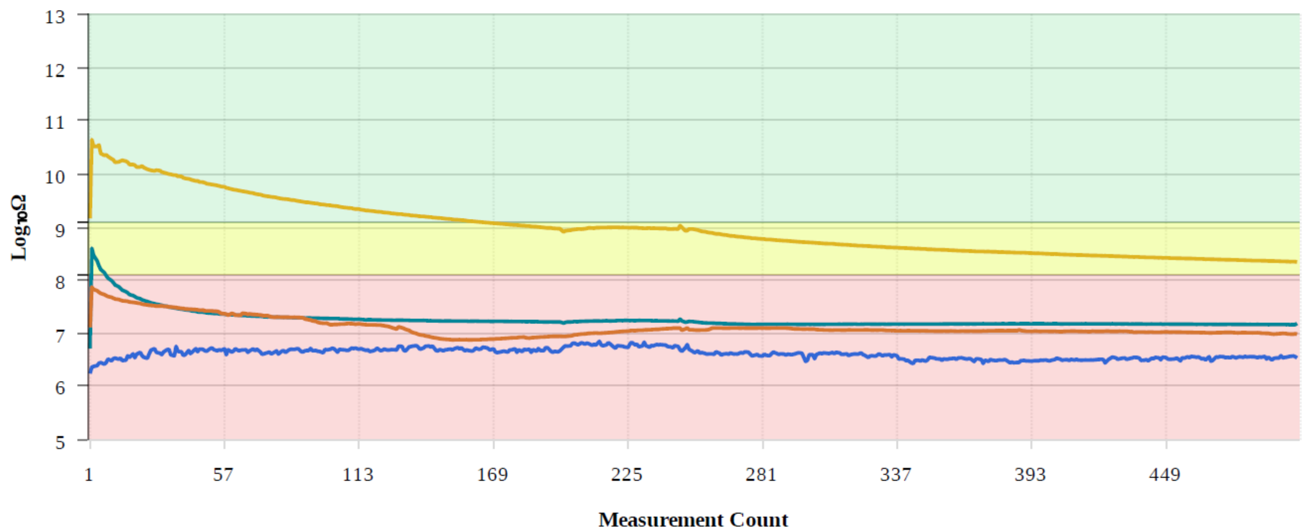

Figure 4: SIR Data Findings for the No-Clean Solder Paste that was not cleaned

Table 1: Measurement Stats for No-Clean Solder Paste that was not cleaned

	Channel A	Channel B	Channel C	Channel D
	7.186 $Log_{10}\Omega$	**6.984 $Log_{10}\Omega$**	**6.537 $Log_{10}\Omega$**	**8.341 $Log_{10}\Omega$**
Measurement Stats				
Maximum:	8.599 $Log_{10}\Omega$	7.866 $Log_{10}\Omega$	6.848 $Log_{10}\Omega$	10.642 $Log_{10}\Omega$
Minimum:	6.714 $Log_{10}\Omega$	6.876 $Log_{10}\Omega$	6.245 $Log_{10}\Omega$	8.345 $Log_{10}\Omega$
Mean:	7.329 $Log_{10}\Omega$	7.162 $Log_{10}\Omega$	6.625 $Log_{10}\Omega$	9.381 $Log_{10}\Omega$
Median:	7.203 $Log_{10}\Omega$	7.049 $Log_{10}\Omega$	6.612 $Log_{10}\Omega$	8.928 $Log_{10}\Omega$
Std Dev:	7.439 $Log_{10}\Omega$	6.960 $Log_{10}\Omega$	5.980 $Log_{10}\Omega$	9.683 $Log_{10}\Omega$
Measurement Info				
Measurement Count:	503	503	503	503
Measurement Errors:	0	0	0	0
First Failure Detected:	Fri, June 28 10:51:49 PM CDT	Fri, June 28 10:51:49 PM CDT	Fri, June 28 10:51:49 PM CDT	
Elapsed Time:	0.16 hours	0.16 hours	0.16 hours	

Figure 5: SIR Measurement Stats for the No-Clean Solder Paste that was not cleaned

Inline Cleaning Process:

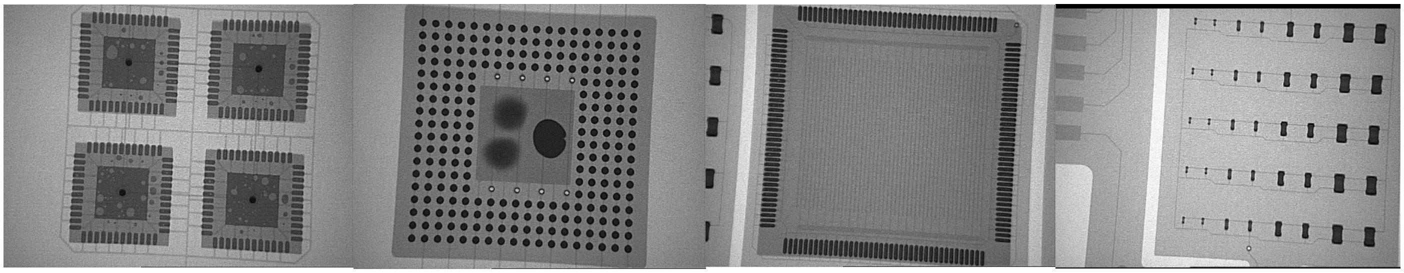

Figure 6: X-Ray Images of the No-Cleaned Solder Paste after cleaning through the Inline Process

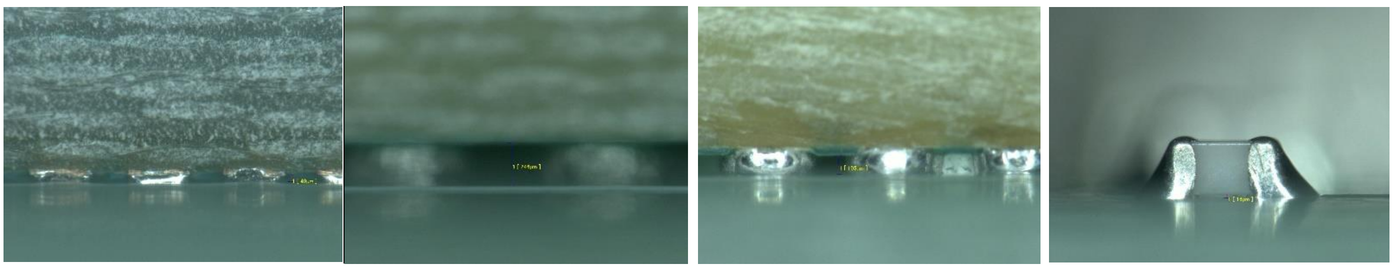

Figure 7: Side views of the No-Clean Solder paste after cleaning through the Inline Process

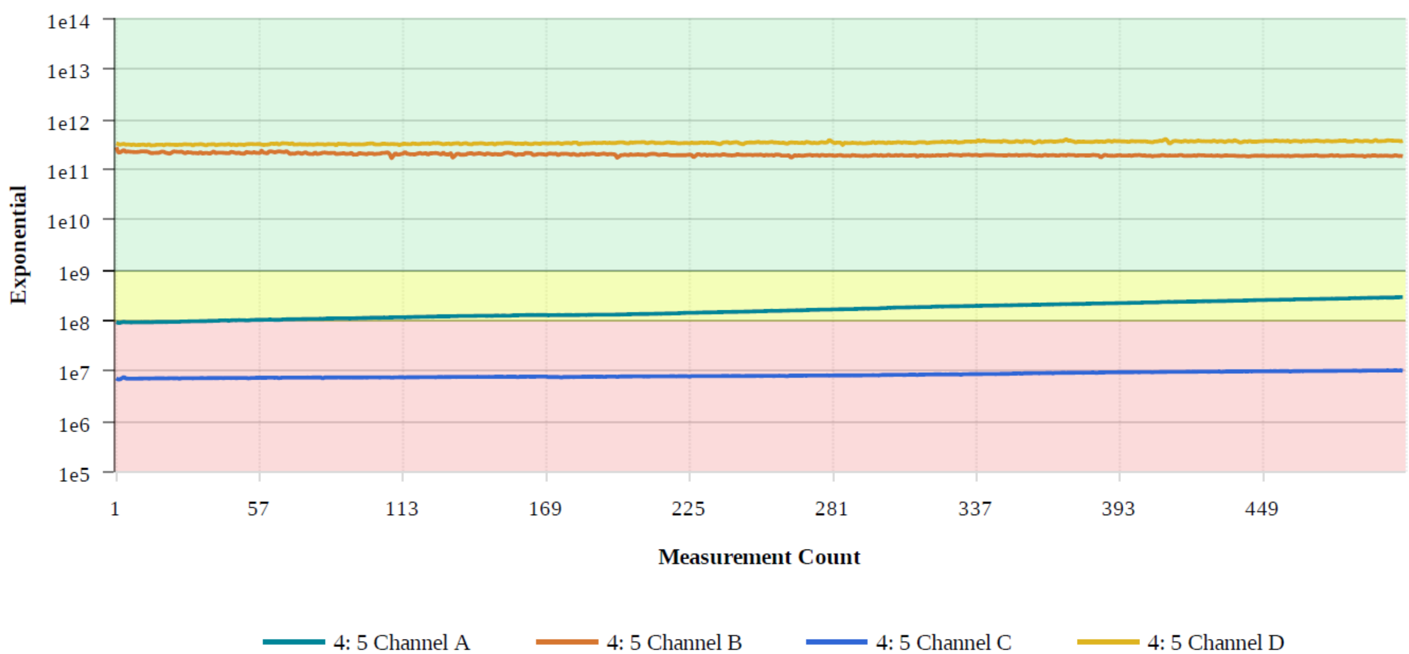

Figure 8: SIR Testing over 168 hours on the No-Clean Solder Paste cleaned through the Inline Process

Table 2: Measurement Stats for No-Clean Solder Paste cleaned through the Inline Process

	Channel A	Channel B	Channel C	Channel D
	2.924855e+8 Ω	1.849362e+11 Ω	1.011739e+7 Ω	3.753049e+11 Ω
Measurement Stats				
Maximum:	2.925634e+8 Ω	2.791126e+11 Ω	1.027399e+7 Ω	4.091766e+11 Ω
Minimum:	9.043414e+7 Ω	1.696844e+11 Ω	6.768718e+6 Ω	3.029382e+11 Ω
Mean:	1.688760e+8 Ω	2.000968e+11 Ω	8.333576e+6 Ω	3.445580e+11 Ω
Median:	1.535458e+8 Ω	1.957368e+11 Ω	7.975566e+6 Ω	3.435247e+11 Ω
Std Dev:	5.787380e+7 Ω	1.248680e+10 Ω	9.715629e+5 Ω	2.063867e+10 Ω
Measurement Info				
Measurement Count:	503	503	503	503
Measurement Errors:	0	0	0	0
First Failure Detected:	Mon, June 24 9:46:07 AM CDT		Mon, June 24 9:46:07 AM CDT	
Elapsed Time:	0.07 hours		0.07 hours	

Figure 9: SIR Measurement Stats on No-Clean Solder Paste cleaned through the Inline process

Batch Cleaning Process

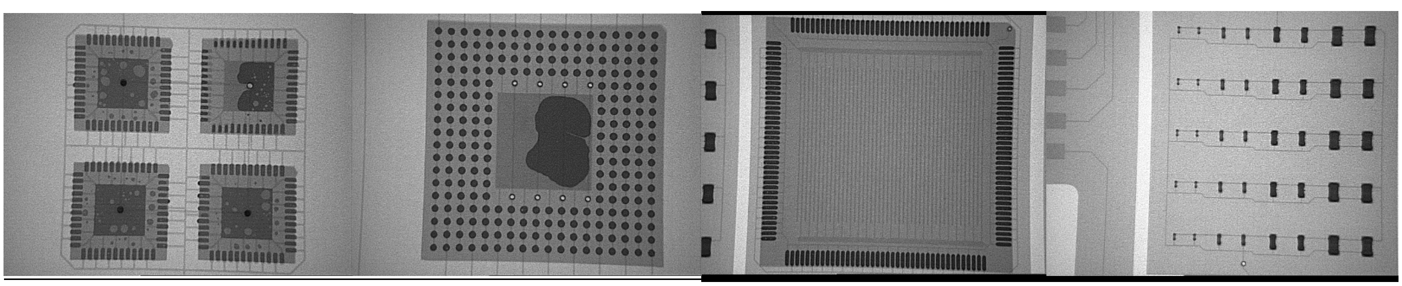

Figure 9: X-Ray Images of the No-Clean Solder Paste after cleaning through the Batch Process

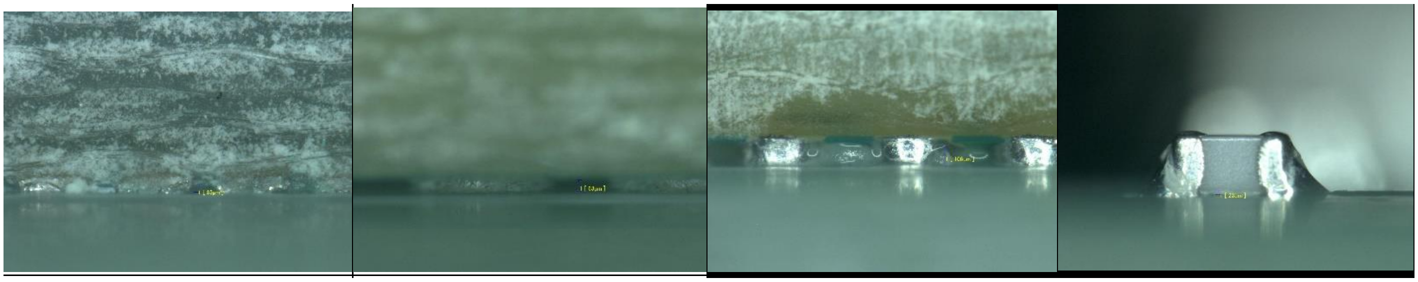

Figure 10: Side views of the No-Clean Solder paste after cleaning through the Batch Process

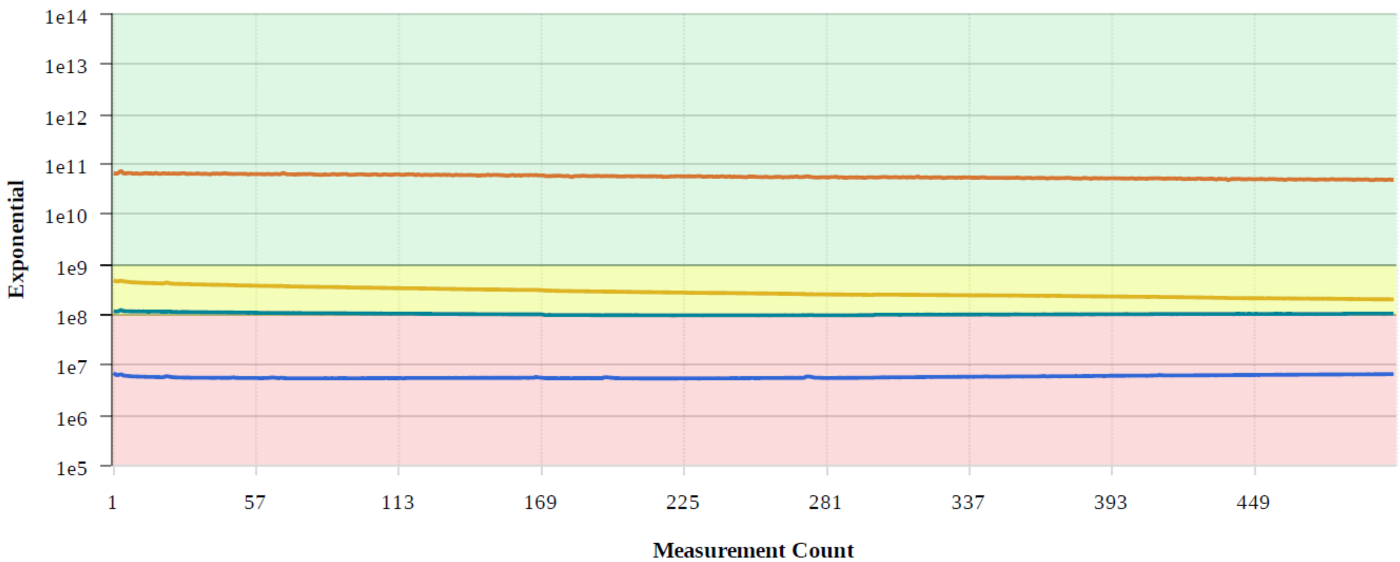

Figure 11: SIR Testing over 168 hours on the No-Clean Solder Paste cleaned through the Batch Process

Table 3: Measurement Stats for the No-Clean Solder Paste cleaned through the Batch Process

	Channel A	Channel B	Channel C	Channel D
	1.058881e+8 Ω	4.936672e+10 Ω	6.601460e+6 Ω	2.043162e+8 Ω
Measurement Stats				
Maximum:	1.253459e+8 Ω	7.434124e+10 Ω	6.930341e+6 Ω	4.881515e+8 Ω
Minimum:	9.759881e+7 Ω	4.858507e+10 Ω	5.402132e+6 Ω	2.034128e+8 Ω
Mean:	1.039583e+8 Ω	5.738689e+10 Ω	5.780623e+6 Ω	2.878636e+8 Ω
Median:	1.034343e+8 Ω	5.666239e+10 Ω	5.591077e+6 Ω	2.693189e+8 Ω
Std Dev:	4.883179e+6 Ω	5.073193e+9 Ω	3.592278e+5 Ω	6.573900e+7 Ω
Measurement Info				
Measurement Count:	503	503	503	503
Measurement Errors:	0	0	0	0
First Failure Detected:	Wed, June 26 6:25:35 PM CDT		Mon, June 24 9:46:07 AM CDT	
Elapsed Time:	56.73 hours		0.07 hours	

No-Clean Solder Paste + Jet Printing Solder Paste in Quadrant 2

Not Cleaned

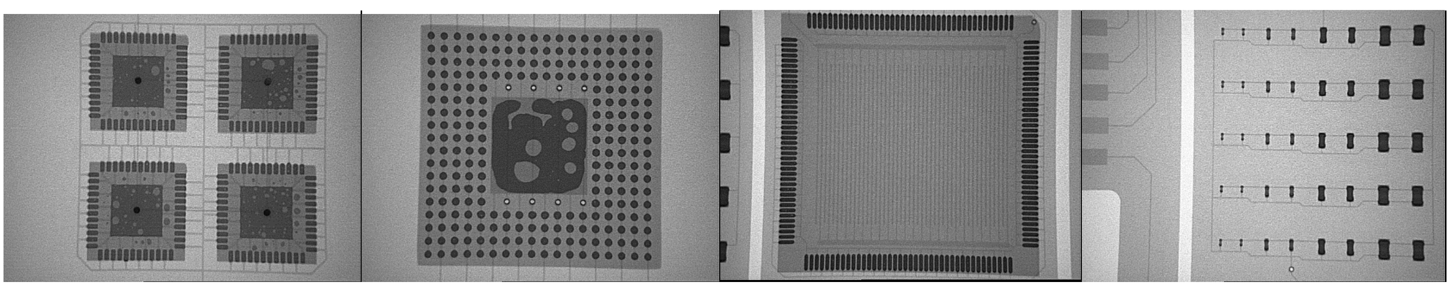

Figure 12: X-Ray Images of the No-Clean + Jet Printing Solder Pastes Not Cleaned

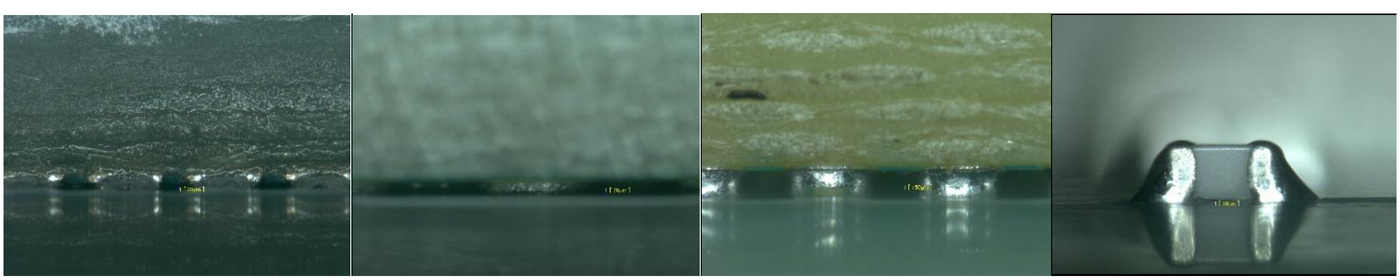

Figure 13: Side views of the No-Clean + Jet Printing Solder pastes Not Cleaned

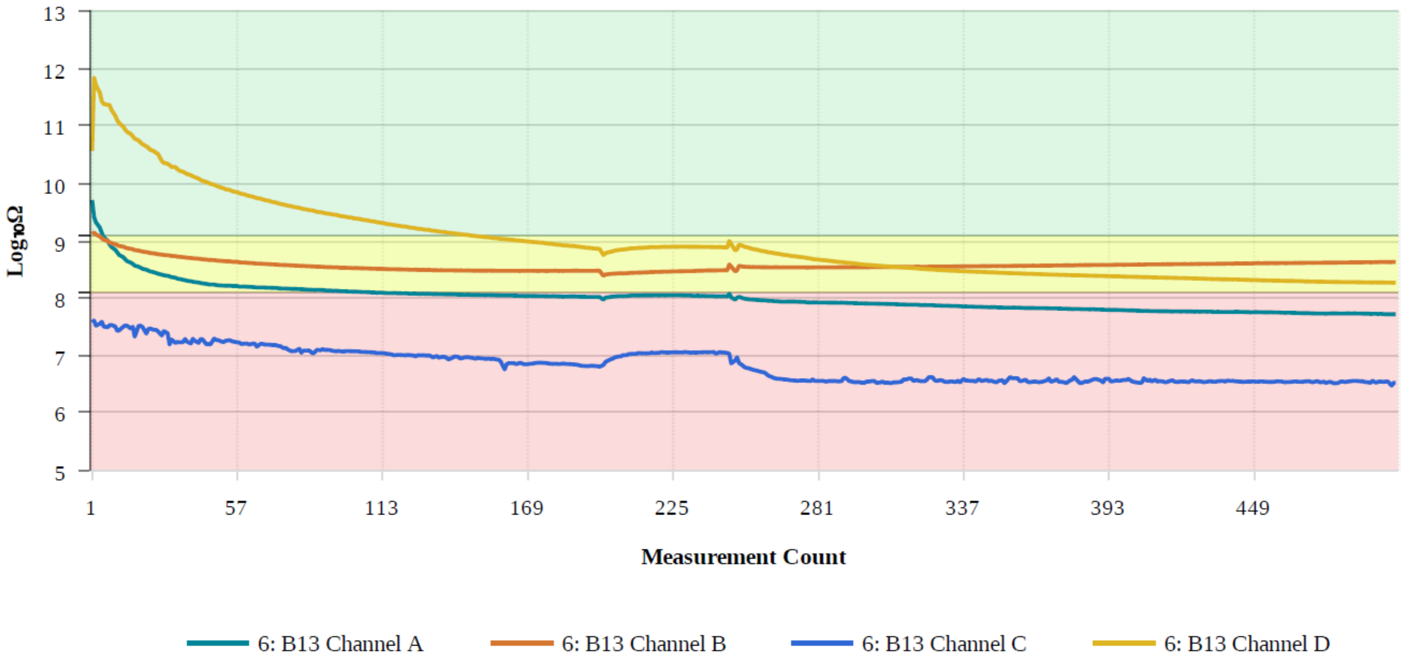

Figure 14: SIR Testing over 168 hours on the No-Clean Solder + Jet Printing Solder Pastes Not Cleaned

Table 4: Measurement Stats for No-Clean and Jet Printed Solder Pastes that was Not Cleaned

	Channel A	**Channel B**	**Channel C**	**Channel D**
	7.719 $Log_{10}\Omega$	**8.629 $Log_{10}\Omega$**	**6.524 $Log_{10}\Omega$**	**8.267 $Log_{10}\Omega$**
Measurement Stats				
Maximum:	9.705 $Log_{10}\Omega$	9.141 $Log_{10}\Omega$	7.608 $Log_{10}\Omega$	11.837 $Log_{10}\Omega$
Minimum:	7.717 $Log_{10}\Omega$	8.386 $Log_{10}\Omega$	6.474 $Log_{10}\Omega$	8.266 $Log_{10}\Omega$
Mean:	8.142 $Log_{10}\Omega$	8.584 $Log_{10}\Omega$	6.933 $Log_{10}\Omega$	9.959 $Log_{10}\Omega$
Median:	7.979 $Log_{10}\Omega$	8.552 $Log_{10}\Omega$	6.792 $Log_{10}\Omega$	8.829 $Log_{10}\Omega$
Std Dev:	8.469 $Log_{10}\Omega$	8.120 $Log_{10}\Omega$	6.849 $Log_{10}\Omega$	10.681 $Log_{10}\Omega$
Measurement Info				
Measurement Count:	503	503	503	503
Measurement Errors:	0	0	0	1
First Failure Detected:	Mon, July 1 4:32:46 PM CDT		Fri, June 28 10:51:49 PM CDT	
Elapsed Time:	65.84 hours		0.16 hours	

Inline Cleaning Process

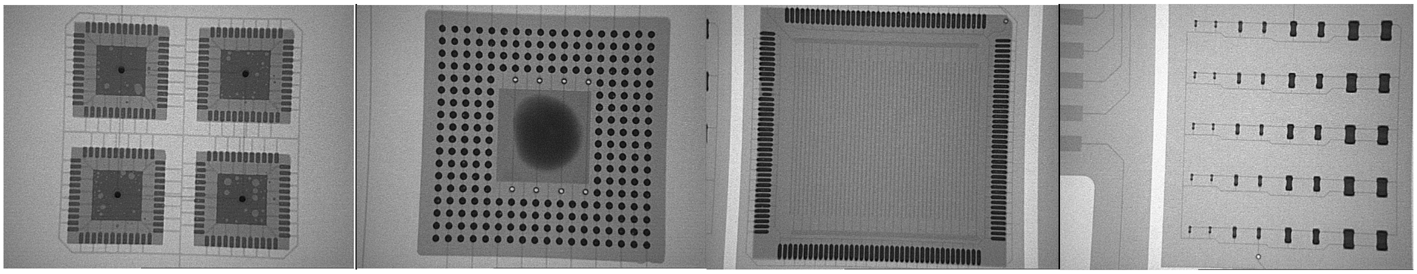

Figure 15: X-Ray Images of the No-Clean + Jet Printing Solder Pastes cleaned through the Inline Process

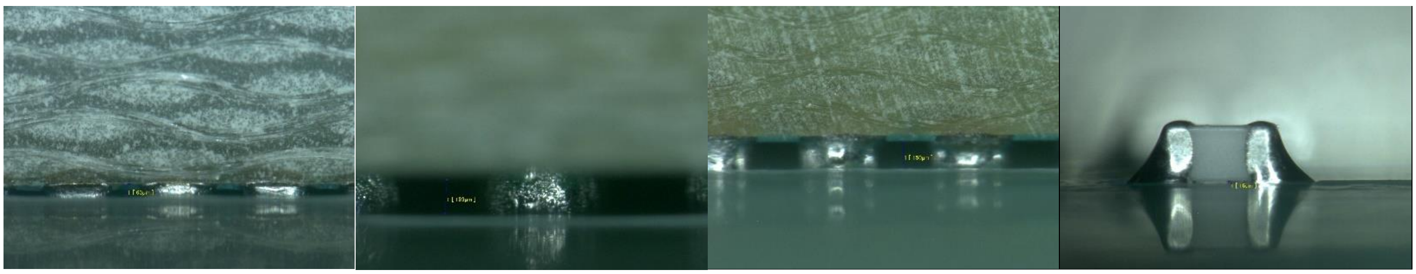

Figure 16: Side views of the No-Clean + Jet Printing Solder Pastes cleaned through the Inline Process

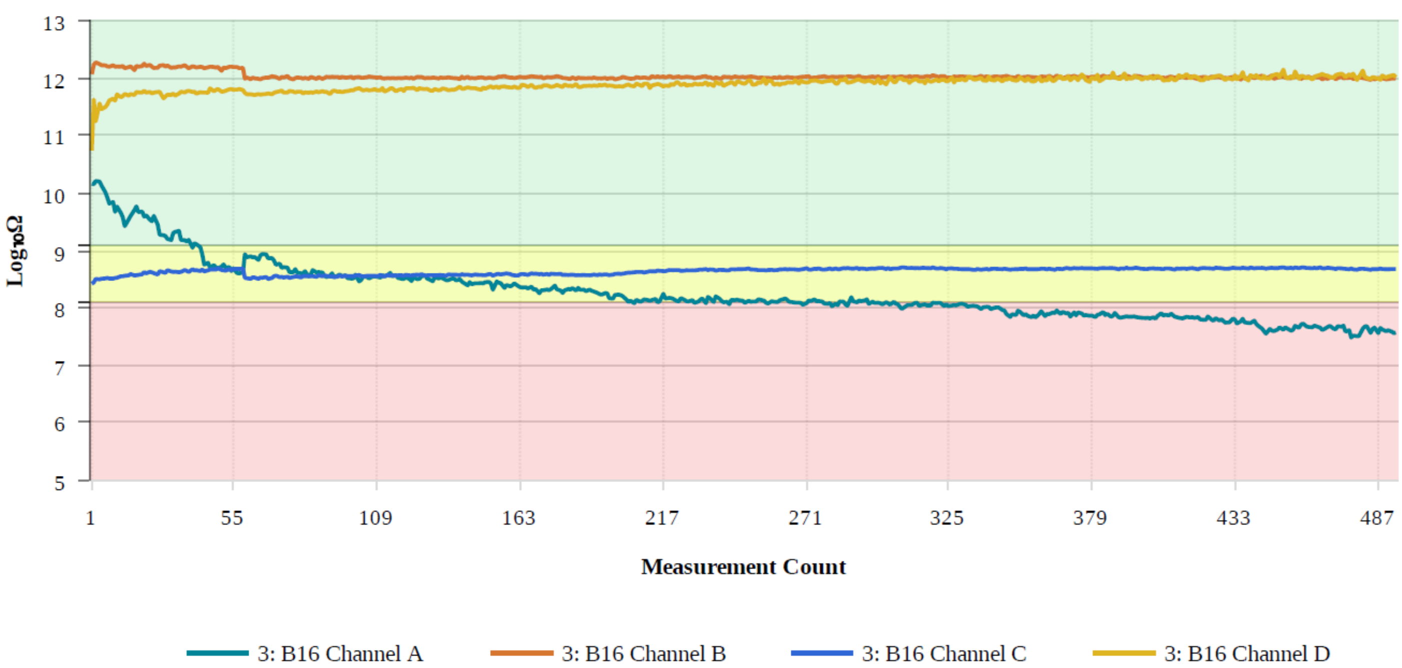

Figure 17: SIR Testing over 168 hours on the No-Clean Solder + Jet Printing Solder Pastes Cleaned through the Inline

Table 5: Measurement Stats for the No-Clean and Jet Printed Solder Pastes cleaned through the Inline Process

	Channel A	Channel B	Channel C	Channel D
	7.56 $Log_{10}\Omega$	11.99 $Log_{10}\Omega$	8.67 $Log_{10}\Omega$	12.01 $Log_{10}\Omega$
Measurement Stats				
Maximum:	10.20 $Log_{10}\Omega$	12.27 $Log_{10}\Omega$	8.70 $Log_{10}\Omega$	12.14 $Log_{10}\Omega$
Minimum:	7.48 $Log_{10}\Omega$	11.96 $Log_{10}\Omega$	8.42 $Log_{10}\Omega$	10.73 $Log_{10}\Omega$
Mean:	8.76 $Log_{10}\Omega$	12.03 $Log_{10}\Omega$	8.63 $Log_{10}\Omega$	11.90 $Log_{10}\Omega$
Median:	8.11 $Log_{10}\Omega$	12.01 $Log_{10}\Omega$	8.66 $Log_{10}\Omega$	11.90 $Log_{10}\Omega$
Std Dev:	9.25 $Log_{10}\Omega$	11.25 $Log_{10}\Omega$	7.74 $Log_{10}\Omega$	11.29 $Log_{10}\Omega$
Measurement Info				
Measurement Count:	493	493	493	493
Measurement Errors:	0	0	0	0
First Failure Detected:	Wed, July 3 05:12:13 CDT			
Elapsed Time:	102.15 hours			

Batch Cleaning Process

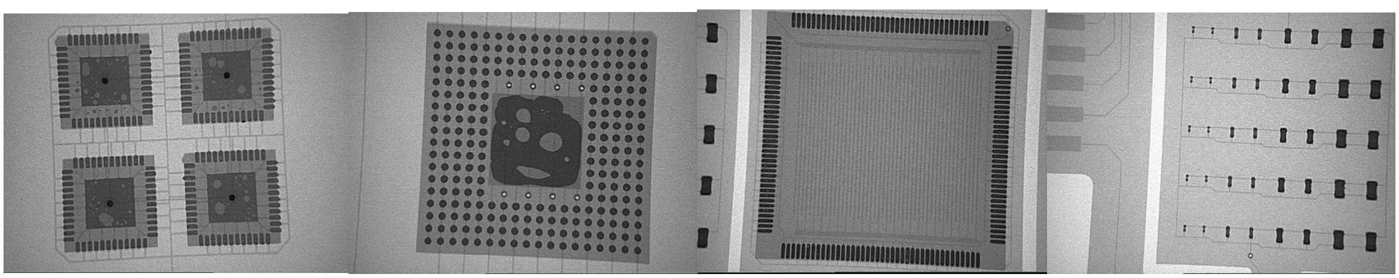

Figure 18: X-Ray Images of the No-Clean + Jet Printing Solder Pastes cleaned through the Batch Process

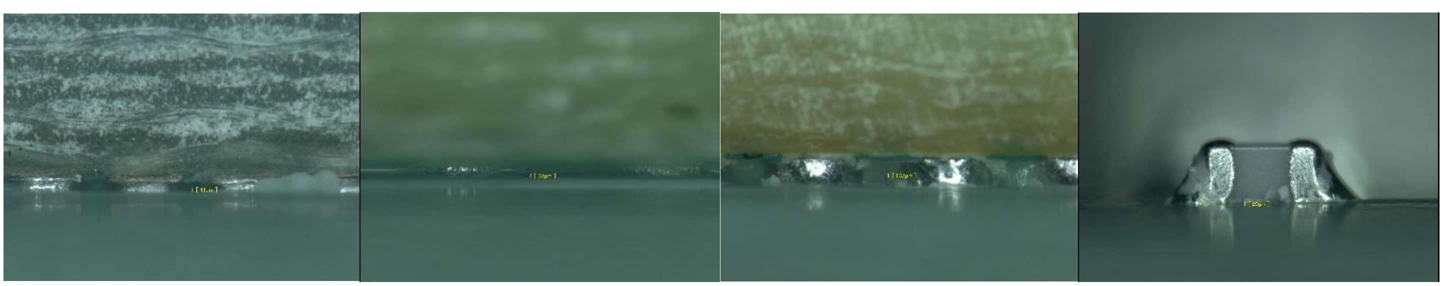

Figure 19: Side views of the No-Clean + Jet Printing Solder Pastes cleaned through the Batch Process

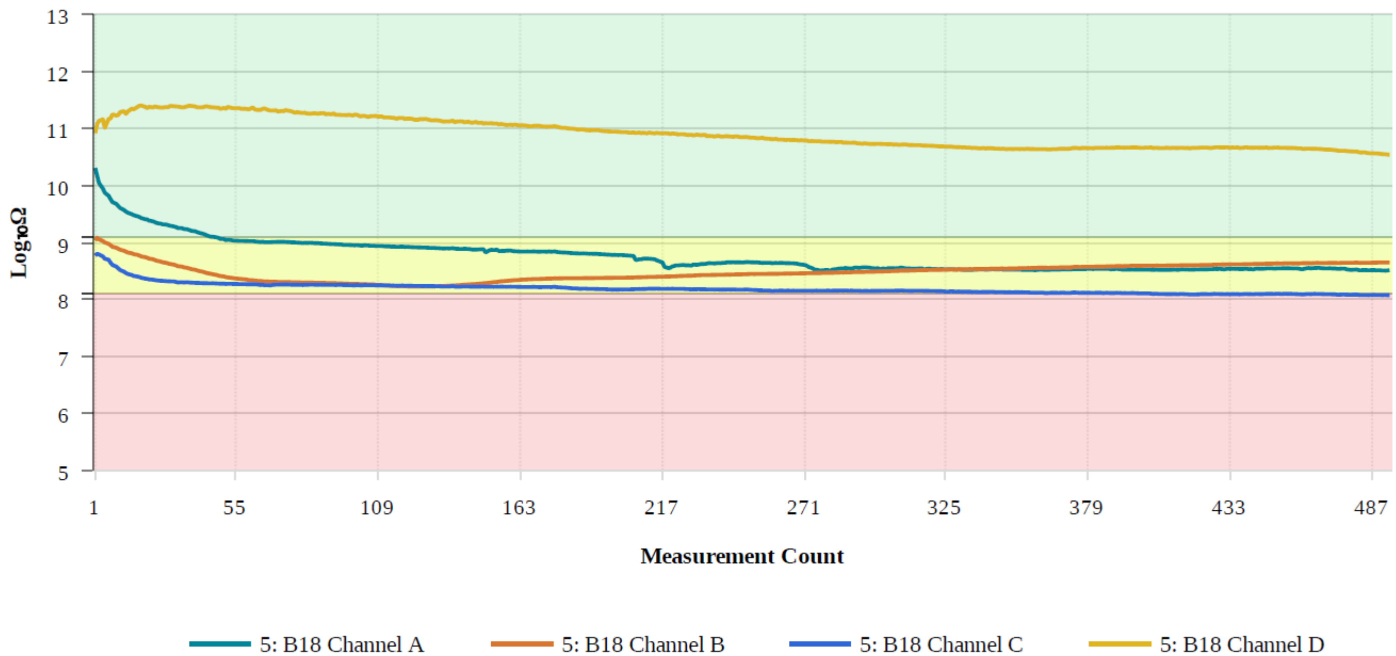

Figure 20: SIR Testing over 168 hours on the No-Clean Solder + Jet Printing Solder Pastes Cleaned through the Batch

Table 6: Measurement Stats for the No-Clean and Jet Printed Solder Pastes cleaned through the Batch Process

	Channel A	Channel B	Channel C	Channel D
	8.51 $\text{Log}_{10}\Omega$	8.64 $\text{Log}_{10}\Omega$	8.07 $\text{Log}_{10}\Omega$	10.53 $\text{Log}_{10}\Omega$
Measurement Stats				
Maximum:	10.30 $\text{Log}_{10}\Omega$	9.07 $\text{Log}_{10}\Omega$	8.79 $\text{Log}_{10}\Omega$	11.39 $\text{Log}_{10}\Omega$
Minimum:	8.50 $\text{Log}_{10}\Omega$	8.22 $\text{Log}_{10}\Omega$	8.07 $\text{Log}_{10}\Omega$	10.53 $\text{Log}_{10}\Omega$
Mean:	8.91 $\text{Log}_{10}\Omega$	8.50 $\text{Log}_{10}\Omega$	8.20 $\text{Log}_{10}\Omega$	10.98 $\text{Log}_{10}\Omega$
Median:	8.63 $\text{Log}_{10}\Omega$	8.47 $\text{Log}_{10}\Omega$	8.16 $\text{Log}_{10}\Omega$	10.84 $\text{Log}_{10}\Omega$
Std Dev:	9.15 $\text{Log}_{10}\Omega$	8.13 $\text{Log}_{10}\Omega$	7.76 $\text{Log}_{10}\Omega$	10.79 $\text{Log}_{10}\Omega$
Measurement Info				
Measurement Count:	493	493	493	493
Measurement Errors:	0	0	0	4

__Water Soluble Solder Paste__

Not Cleaned

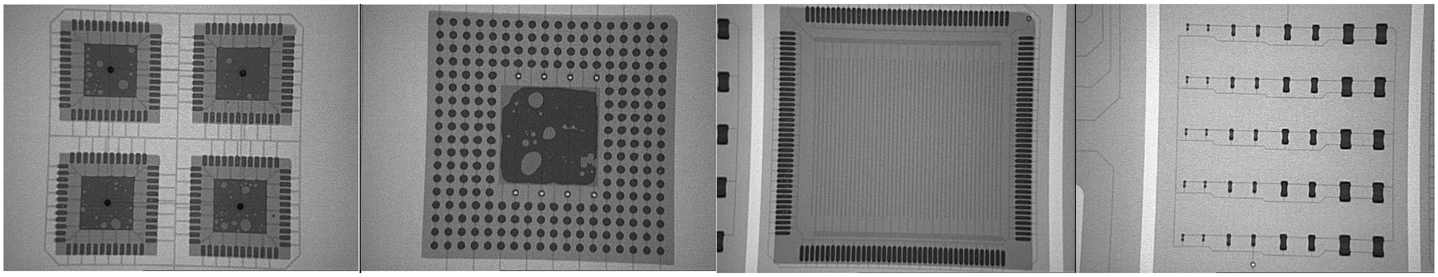

Figure 21: X-Ray Images of the Water Soluble Solder Paste that was not cleaned

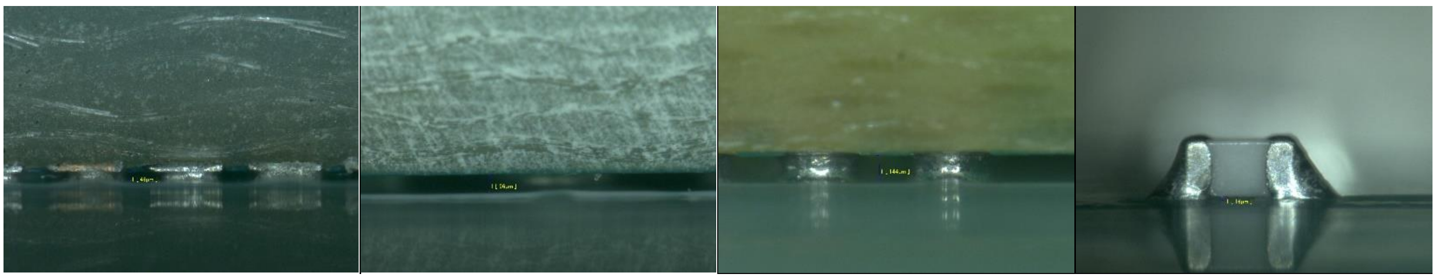

Figure 22: Side views of the Water Soluble Solder Pastes that was not cleaned

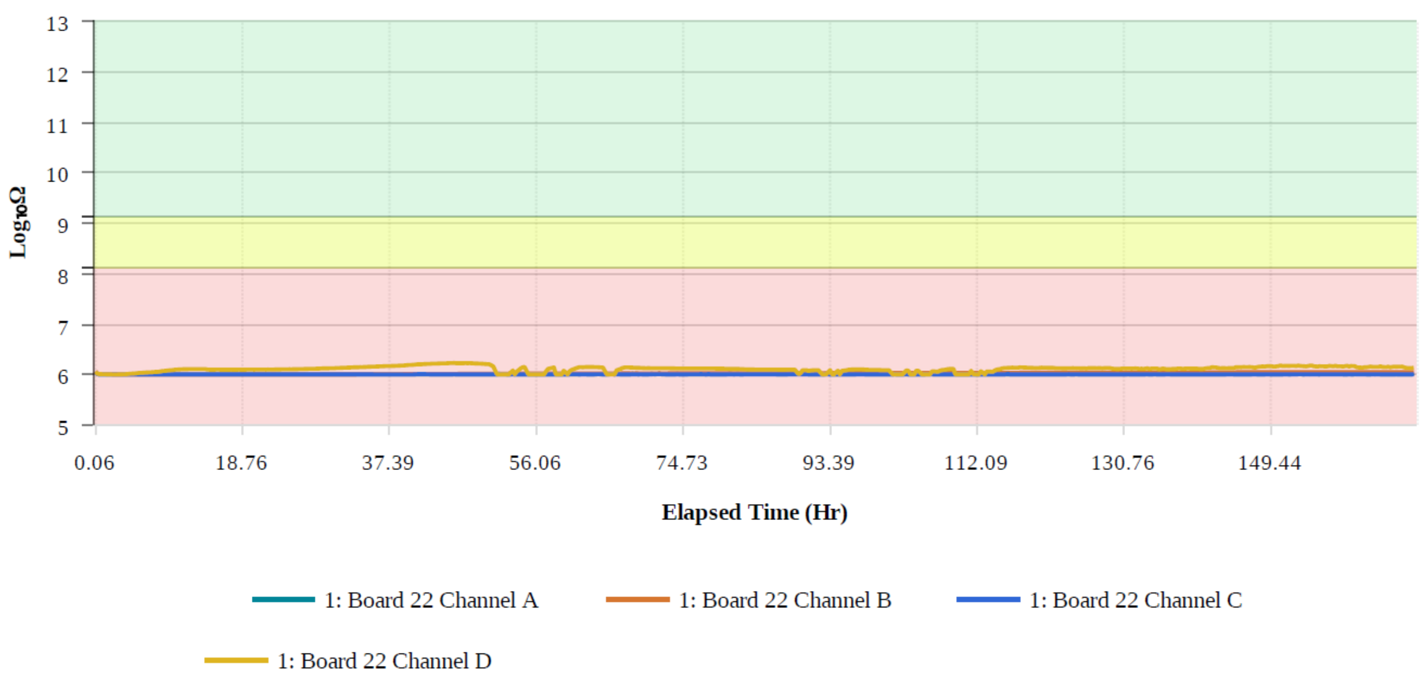

Figure 23: SIR Testing over 168 hours on the Water Soluble Solder Paste that was Not Cleaned

Table 7: Measurement Stats for the Water Soluble Solder Paste that was Not Cleaned

	Channel A	Channel B	Channel C	Channel D
	6.020 $Log_{10}\Omega$	6.041 $Log_{10}\Omega$	5.997 $Log_{10}\Omega$	6.130 $Log_{10}\Omega$
Measurement Stats				
Maximum:	6.033 $Log_{10}\Omega$	6.055 $Log_{10}\Omega$	6.037 $Log_{10}\Omega$	6.224 $Log_{10}\Omega$
Minimum:	5.995 $Log_{10}\Omega$	5.995 $Log_{10}\Omega$	5.997 $Log_{10}\Omega$	5.997 $Log_{10}\Omega$
Mean:	5.999 $Log_{10}\Omega$	6.020 $Log_{10}\Omega$	5.998 $Log_{10}\Omega$	6.109 $Log_{10}\Omega$
Median:	5.998 $Log_{10}\Omega$	6.022 $Log_{10}\Omega$	5.998 $Log_{10}\Omega$	6.113 $Log_{10}\Omega$
Std Dev:	4.150 $Log_{10}\Omega$	4.561 $Log_{10}\Omega$	3.725 $Log_{10}\Omega$	5.194 $Log_{10}\Omega$
Measurement Info				
Measurement Count:	503	503	503	503
Measurement Errors:	0	0	0	0
First Failure Detected:	Fri, June 21 1:46:22 PM CDT	Fri, June 21 1:46:22 PM CDT	Fri, June 21 1:46:22 PM CDT	Fri, June 21 1:46:22 PM CDT
Elapsed Time:	0.06 hours	0.06 hours	0.06 hours	0.06 hours

Inline Cleaning Process

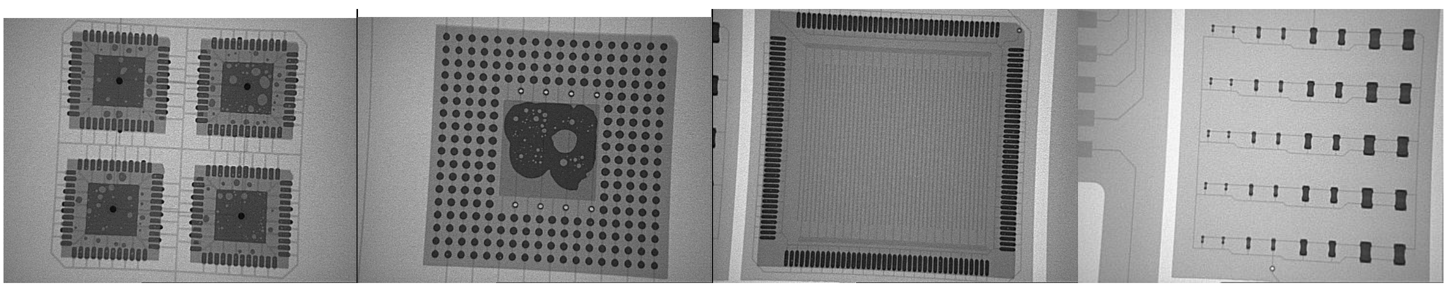

Figure 24: X-Ray Images of the Water Soluble Solder Paste cleaned through the Inline Process

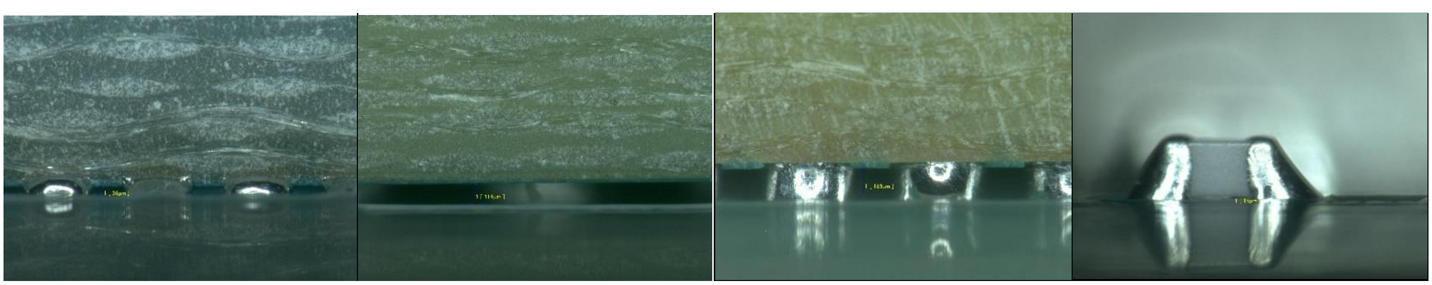

Figure 25: Side views of the Water Soluble Solder Pastes cleaned through the Inline Process

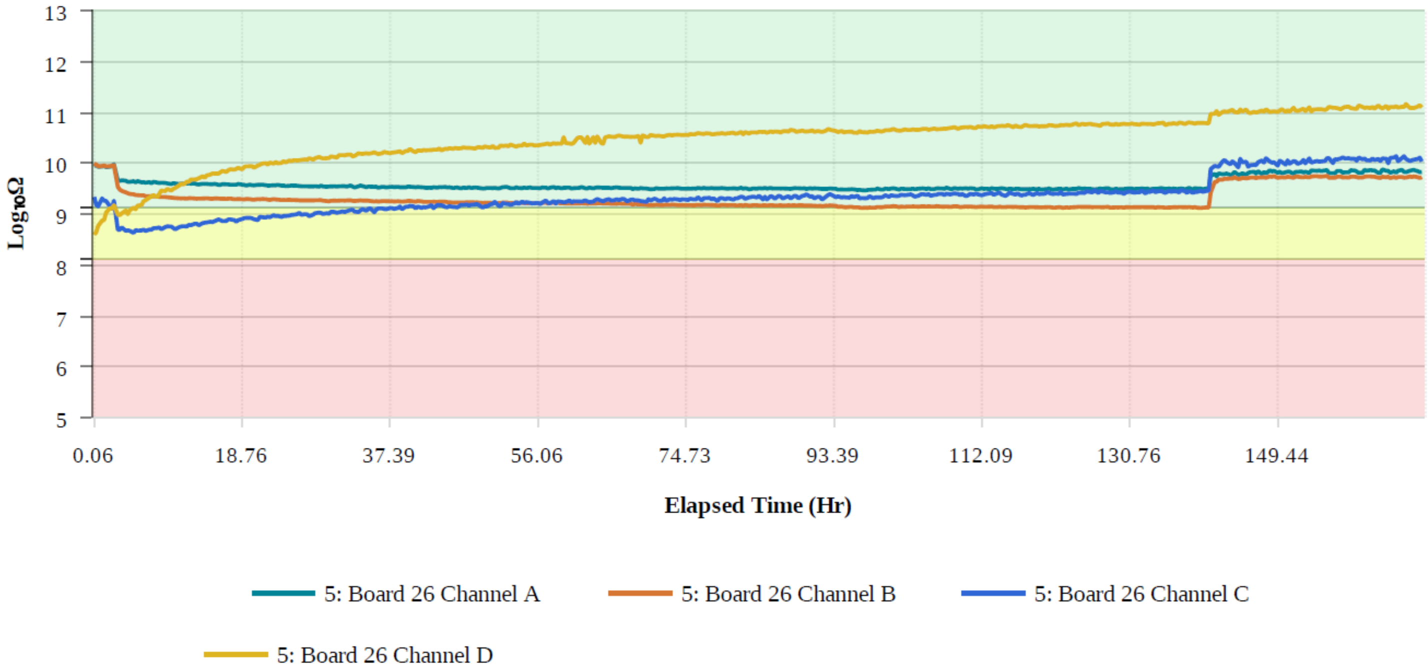

Figure 26: SIR Testing over 168 hours on the Water Soluble Solder Paste cleaned through the Inline Process

Table 8: Measurement Stats for the Water Soluble Solder Paste cleaned through the Inline Process

	Channel A	Channel B	Channel C	Channel D
	9.823 $Log_{10}\Omega$	9.721 $Log_{10}\Omega$	10.030 $Log_{10}\Omega$	11.091 $Log_{10}\Omega$
Measurement Stats				
Maximum:	9.974 $Log_{10}\Omega$	9.988 $Log_{10}\Omega$	10.134 $Log_{10}\Omega$	11.158 $Log_{10}\Omega$
Minimum:	9.460 $Log_{10}\Omega$	9.115 $Log_{10}\Omega$	8.625 $Log_{10}\Omega$	8.592 $Log_{10}\Omega$
Mean:	9.594 $Log_{10}\Omega$	9.362 $Log_{10}\Omega$	9.510 $Log_{10}\Omega$	10.649 $Log_{10}\Omega$
Median:	9.510 $Log_{10}\Omega$	9.210 $Log_{10}\Omega$	9.306 $Log_{10}\Omega$	10.598 $Log_{10}\Omega$
Std Dev:	9.150 $Log_{10}\Omega$	9.205 $Log_{10}\Omega$	9.538 $Log_{10}\Omega$	10.543 $Log_{10}\Omega$
Measurement Info				
Measurement Count:	503	503	503	503
Measurement Errors:	0	0	0	0

Batch Cleaning Process

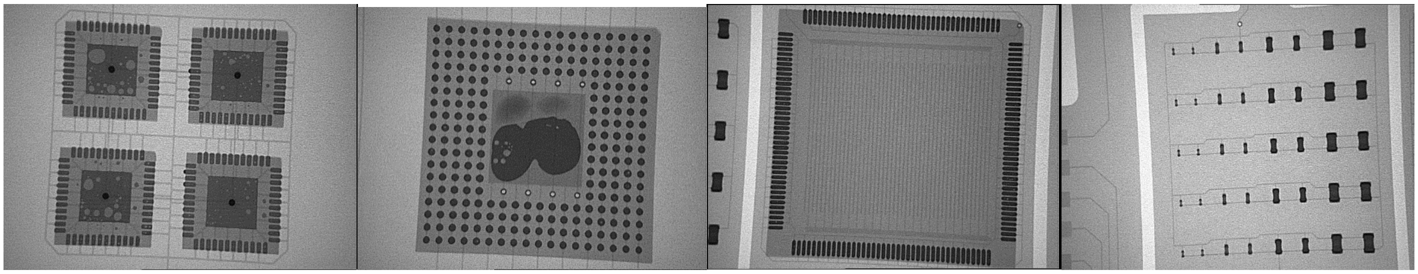

Figure 27: X-Ray Images of the Water Soluble Solder Paste cleaned through the Batch Process

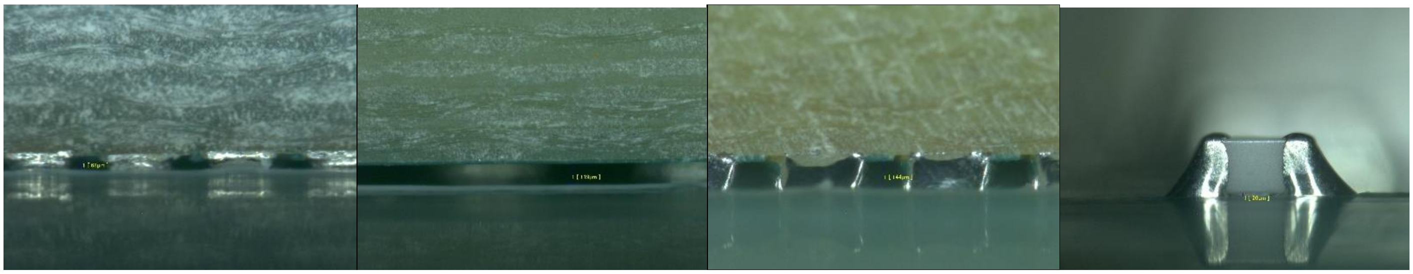

Figure 28: Side views of the Water Soluble Solder Pastes cleaned through the Batch Process

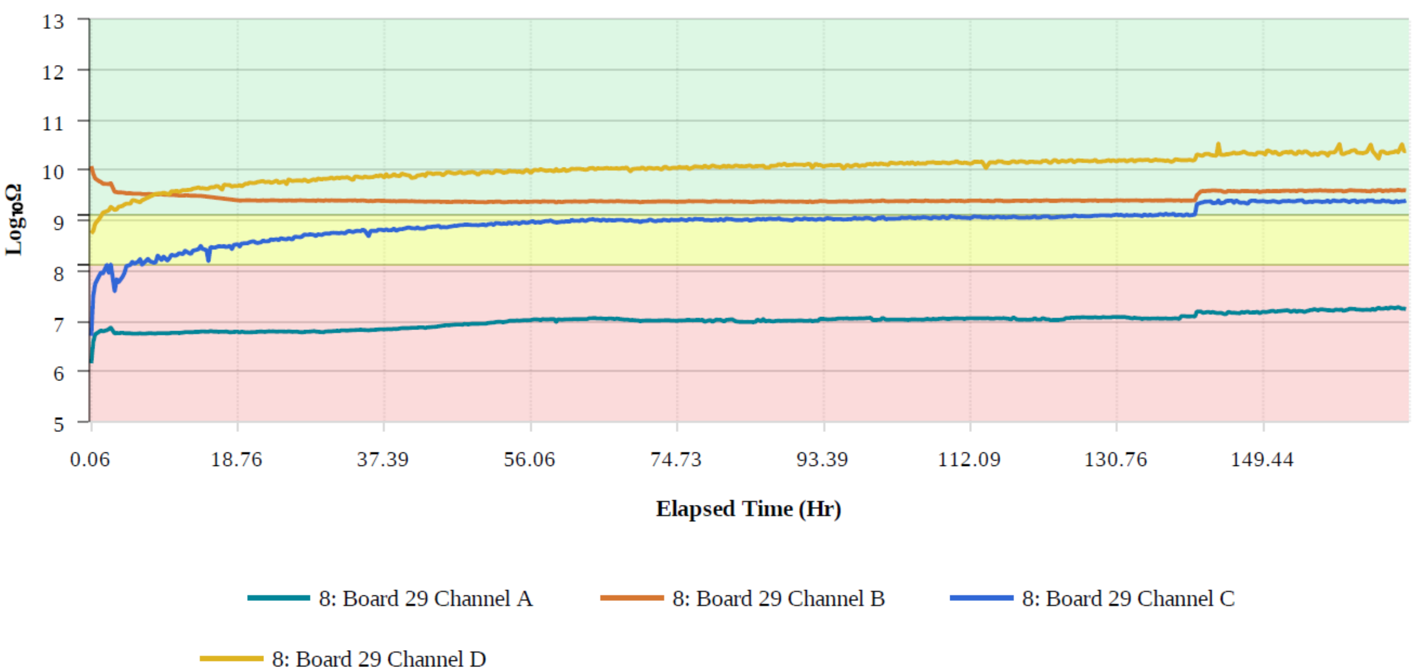

Figure 29: SIR Testing over 168 hours on the Water Soluble Solder Paste cleaned through the Batch Process

Table 9: Measurement Stats for the Water Soluble Solder Paste cleaned through the Batch Process

	Channel A	Channel B	Channel C	Channel D
	7.236 $Log_{10}\Omega$	9.592 $Log_{10}\Omega$	9.392 $Log_{10}\Omega$	10.376 $Log_{10}\Omega$
Measurement Stats				
Maximum:	7.274 $Log_{10}\Omega$	10.073 $Log_{10}\Omega$	9.397 $Log_{10}\Omega$	10.527 $Log_{10}\Omega$
Minimum:	6.162 $Log_{10}\Omega$	9.352 $Log_{10}\Omega$	6.707 $Log_{10}\Omega$	8.745 $Log_{10}\Omega$
Mean:	7.013 $Log_{10}\Omega$	9.443 $Log_{10}\Omega$	9.038 $Log_{10}\Omega$	10.085 $Log_{10}\Omega$
Median:	7.023 $Log_{10}\Omega$	9.387 $Log_{10}\Omega$	9.016 $Log_{10}\Omega$	10.074 $Log_{10}\Omega$
Std Dev:	6.508 $Log_{10}\Omega$	8.913 $Log_{10}\Omega$	8.806 $Log_{10}\Omega$	9.760 $Log_{10}\Omega$
Measurement Info				
Measurement Count:	503	503	503	503
Measurement Errors:	0	15	0	5
First Failure Detected:	Fri, June 21 1:46:22 PM CDT		Fri, June 21 1:46:22 PM CDT	
Elapsed Time:	0.06 hours		0.06 hours	

Water Soluble Solder Paste + Jet Printing Solder Paste

Not Cleaned

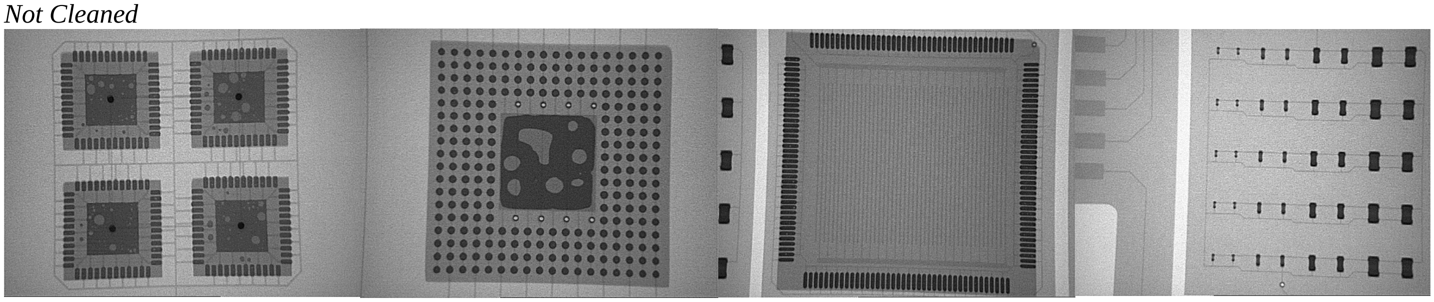

Figure 30: X-Ray Images of the Water Soluble + Jet Printing Solder Pastes that was Not Cleaned

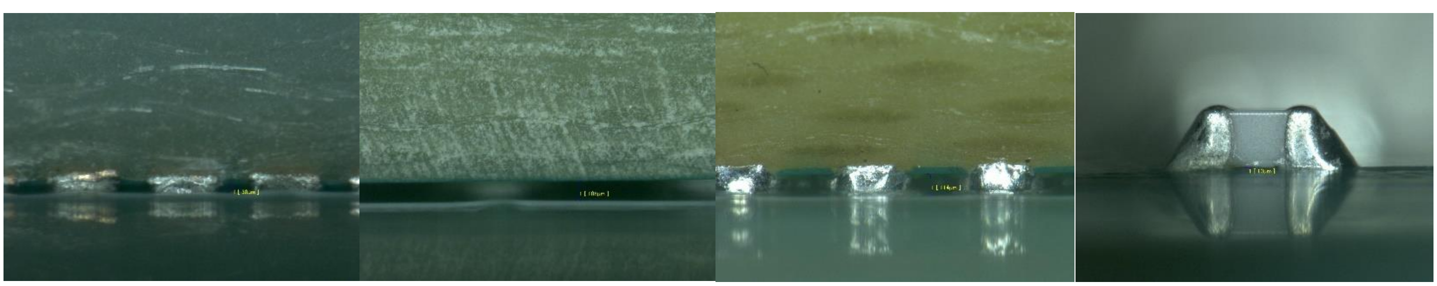

Figure 31: Side views of the Water Soluble + Jet Printing Solder Pastes that was Not Cleaned

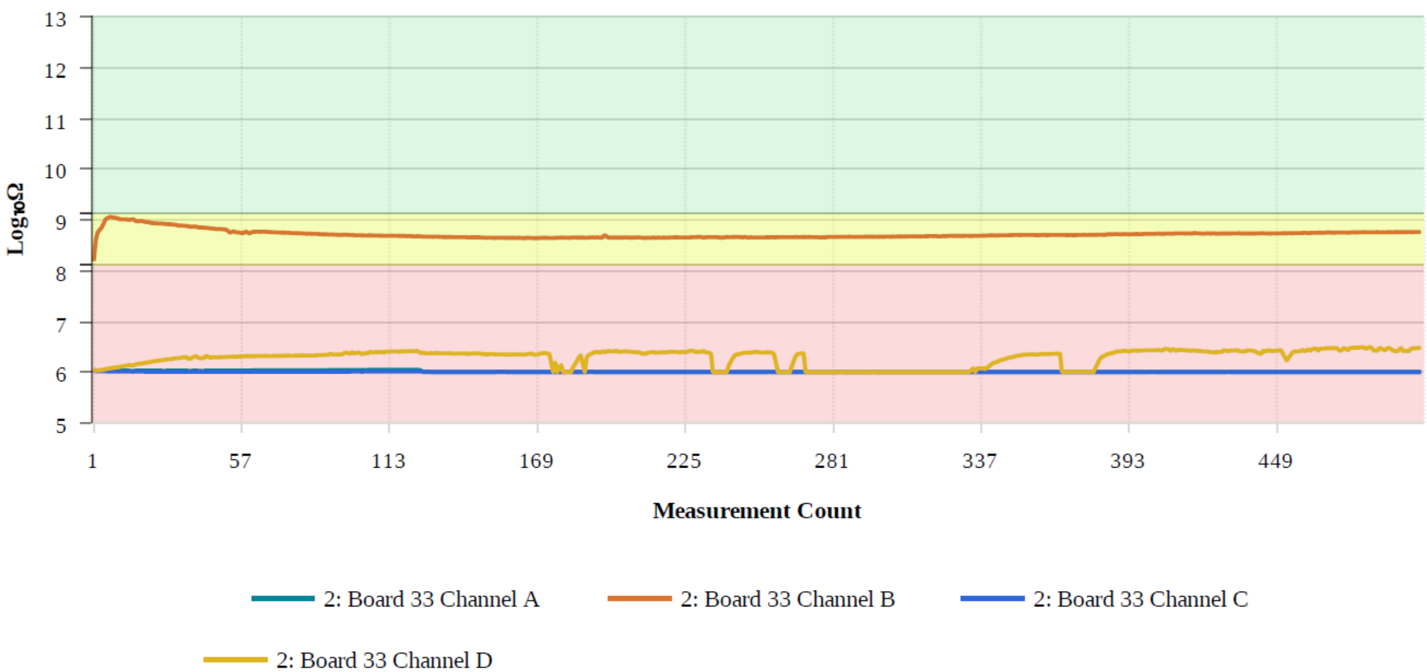

Figure 32: SIR Testing over 168 hours on the Water Soluble + Jet Printing Solder Paste that was Not Cleaned

Table 10: Measurement Stats for the Water Soluble + Jet Printed Solder Pastes that was Not Cleaned

	Channel A	Channel B	Channel C	Channel D
	5.99 $Log_{10}\Omega$	8.75 $Log_{10}\Omega$	5.99 $Log_{10}\Omega$	6.47 $Log_{10}\Omega$
Measurement Stats				
Maximum:	6.05 $Log_{10}\Omega$	9.04 $Log_{10}\Omega$	6.03 $Log_{10}\Omega$	6.48 $Log_{10}\Omega$
Minimum:	5.99 $Log_{10}\Omega$	8.18 $Log_{10}\Omega$	5.99 $Log_{10}\Omega$	5.99 $Log_{10}\Omega$
Mean:	6.00 $Log_{10}\Omega$	8.71 $Log_{10}\Omega$	6.00 $Log_{10}\Omega$	6.30 $Log_{10}\Omega$
Median:	5.99 $Log_{10}\Omega$	8.69 $Log_{10}\Omega$	5.99 $Log_{10}\Omega$	6.34 $Log_{10}\Omega$
Std Dev:	4.55 $Log_{10}\Omega$	8.07 $Log_{10}\Omega$	3.92 $Log_{10}\Omega$	5.79 $Log_{10}\Omega$
Measurement Info				
Measurement Count:	503	503	503	503
Measurement Errors:	0	0	0	0
First Failure Detected:	Fri, June 21 15:09:20 CDT		Fri, June 21 15:09:20 CDT	Fri, June 21 15:09:20 CDT
Elapsed Time:	0.06 hours		0.06 hours	0.06 hours

Inline Cleaning Process

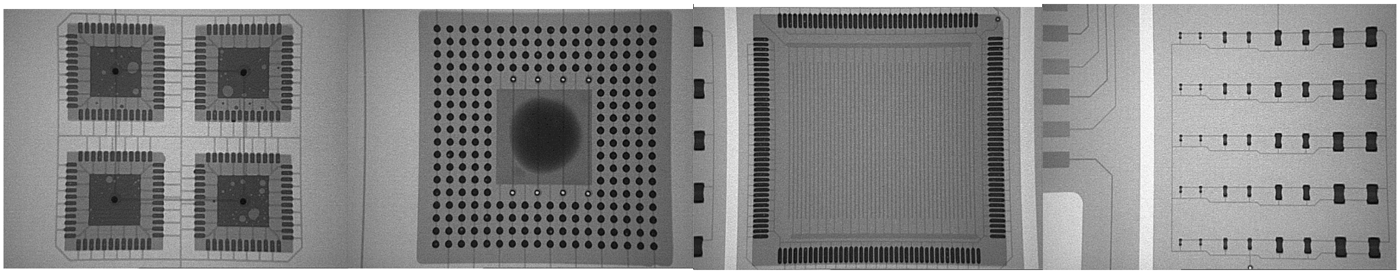

Figure 33: X-Ray Images of the Water Soluble + Jet Printing Solder Pastes cleaned through the Inline Process

Figure 34: Side views of the Water Soluble + Jet Printing Solder Pastes cleaned through the Inline Process

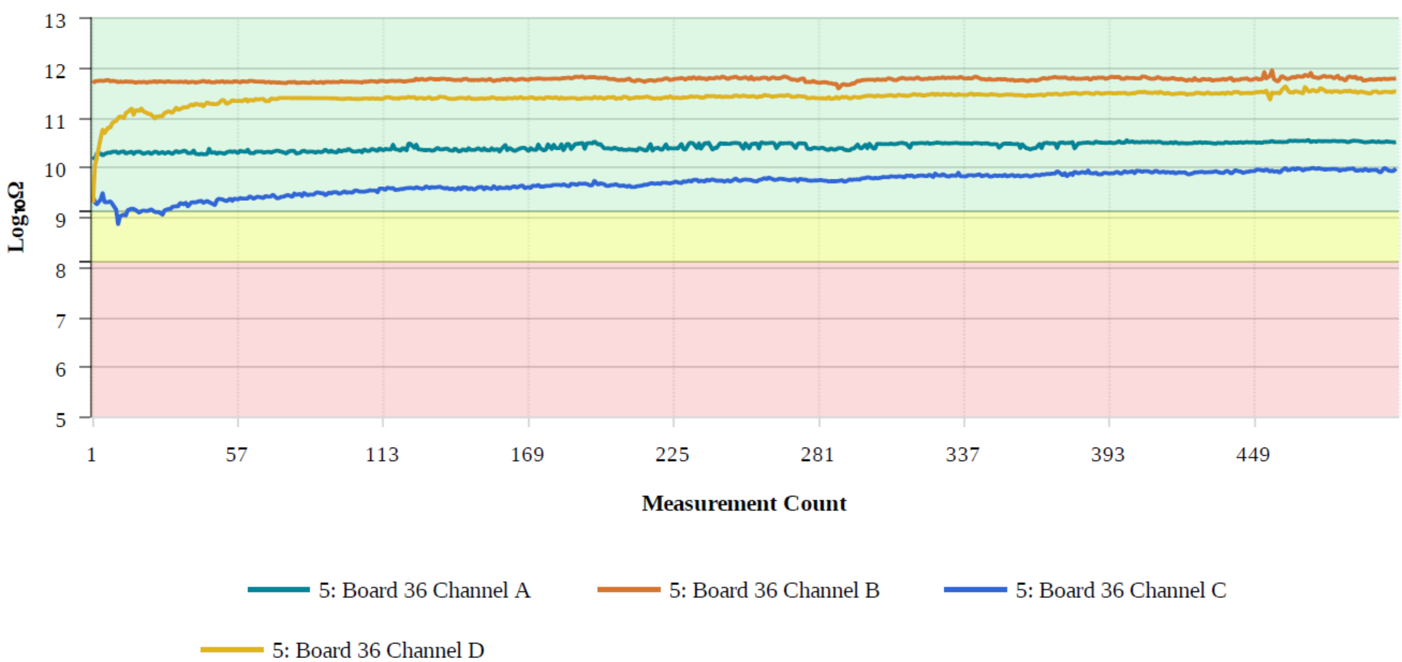

Figure 35

: SIR Testing over 168 hours on the Water Soluble + Jet Printing Solder Paste cleaned through the Inline Process

Table 11: Measurement Stats for the Water Soluble + Jet Printed Solder Pastes cleaned through the Inline Process

	Channel A	Channel B	Channel C	Channel D
	10.51 $Log_{10}\Omega$	11.78 $Log_{10}\Omega$	9.98 $Log_{10}\Omega$	11.51 $Log_{10}\Omega$
Measurement Stats				
Maximum:	10.55 $Log_{10}\Omega$	11.95 $Log_{10}\Omega$	9.99 $Log_{10}\Omega$	11.62 $Log_{10}\Omega$
Minimum:	10.17 $Log_{10}\Omega$	11.58 $Log_{10}\Omega$	8.86 $Log_{10}\Omega$	9.30 $Log_{10}\Omega$
Mean:	10.42 $Log_{10}\Omega$	11.76 $Log_{10}\Omega$	9.73 $Log_{10}\Omega$	11.41 $Log_{10}\Omega$
Median:	10.45 $Log_{10}\Omega$	11.76 $Log_{10}\Omega$	9.73 $Log_{10}\Omega$	11.42 $Log_{10}\Omega$
Std Dev:	9.69 $Log_{10}\Omega$	10.72 $Log_{10}\Omega$	9.36 $Log_{10}\Omega$	10.77 $Log_{10}\Omega$
Measurement Info				
Measurement Count:	503	503	503	503
Measurement Errors:	0	0	0	24

Batch Cleaning Process

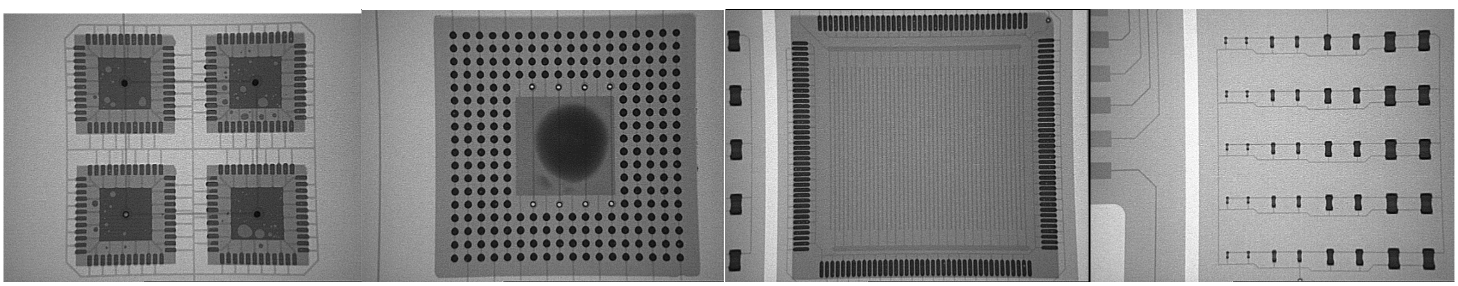

Figure 36: X-Ray Images of the Water Soluble + Jet Printing Solder Pastes cleaned through the Batch Process

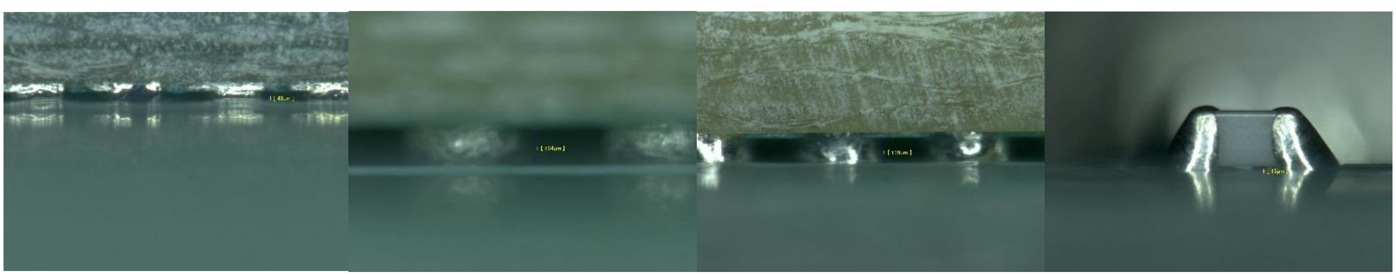

Figure 37: Side views of the Water Soluble + Jet Printing Solder Pastes cleaned through the Batch Process

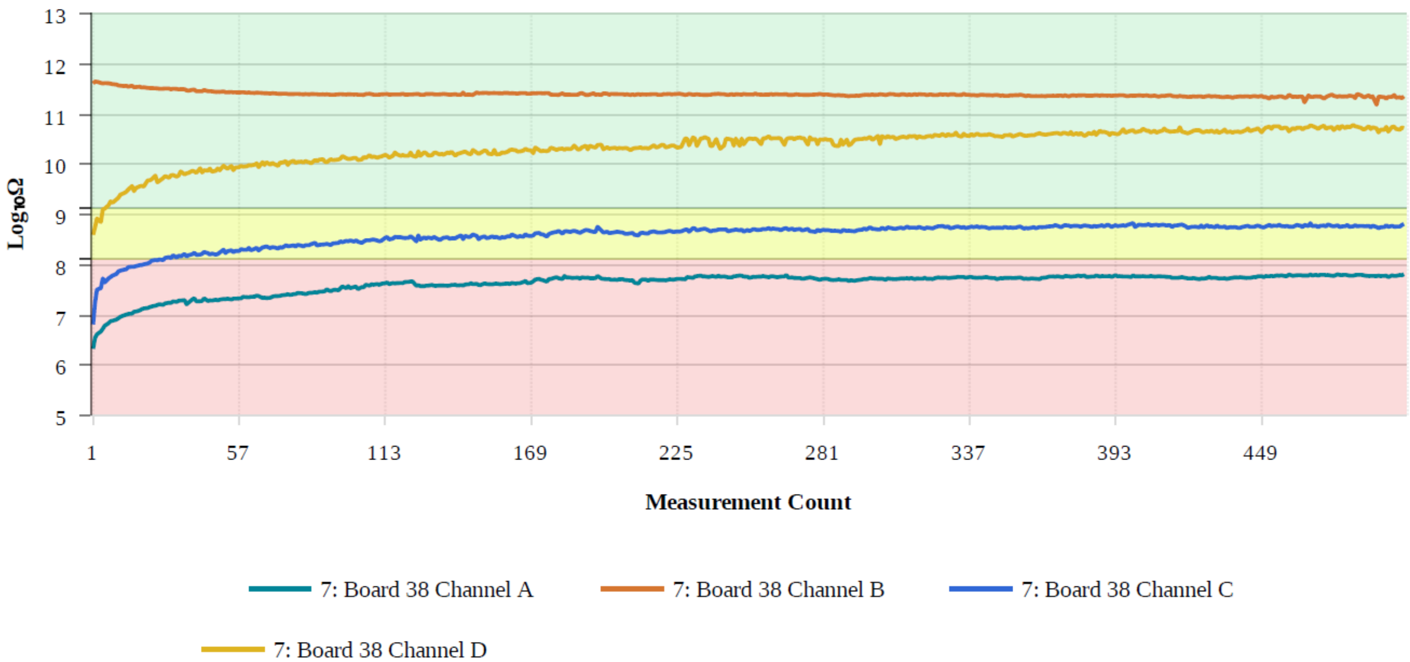

Figure 38: SIR Testing over 168 hours on the Water Soluble + Jet Printing Solder Paste cleaned through the Batch Process

Table 12: Measurement Stats for the Water Soluble + Jet Printed Solder Pastes cleaned through the Batch Process

	Channel A	Channel B	Channel C	Channel D
	7.80 $Log_{10}\Omega$	11.34 $Log_{10}\Omega$	8.80 $Log_{10}\Omega$	10.71 $Log_{10}\Omega$
Measurement Stats				
Maximum:	7.80 $Log_{10}\Omega$	11.64 $Log_{10}\Omega$	8.82 $Log_{10}\Omega$	10.77 $Log_{10}\Omega$
Minimum:	6.32 $Log_{10}\Omega$	11.18 $Log_{10}\Omega$	6.80 $Log_{10}\Omega$	8.59 $Log_{10}\Omega$
Mean:	7.66 $Log_{10}\Omega$	11.39 $Log_{10}\Omega$	8.63 $Log_{10}\Omega$	10.44 $Log_{10}\Omega$
Median:	7.71 $Log_{10}\Omega$	11.38 $Log_{10}\Omega$	8.68 $Log_{10}\Omega$	10.48 $Log_{10}\Omega$
Std Dev:	7.16 $Log_{10}\Omega$	10.54 $Log_{10}\Omega$	8.19 $Log_{10}\Omega$	10.18 $Log_{10}\Omega$
Measurement Info				
Measurement Count:	503	503	503	503
Measurement Errors:	0	3	0	0
First Failure Detected:	Fri, June 21 15:09:20 CDT		Fri, June 21 15:09:20 CDT	
Elapsed Time:	0.06 hours		0.06 hours	

Inferences from the Data Findings

Analysis of covariance (ANCOVA) statistical model was used to analyze the main effects. ANCOVA, which blends Anova and Regression, evaluates whether the means of a dependent variable is equal across levels of a categorical independent variable. The independent variable was statistically controlled for the effects of other nuisance variables.

Just as in ANOVA, there are several ways to analyze the differences in how the variance is partitioned (sum of squares). Types I, II, & & III are common. The analysis makes no consensus on which is “right.” Much of the analysis of this data set was done with Type II sum of squares. This method detects main effects. In addition, Type I analysis was performed on variables that showed lower statistical significance.

Hypothesis testing was used to determine if variation between two sample distributions can be explained through random chance or not. If we have to conclude that two distributions vary in a meaningful way, we must take enough precaution to see that the differences are not just through random chance. At the heart of Type I error (false – positive) is that we don't want to make an unwarranted hypothesis so we exercise a lot of care by minimizing the chance of its occurrence

Effect size measures the impact of each factor from the data findings. The four blocks of data were compared. Most effect sizes ranged from 0-1. These varieties are extensions of the linear regression. This form of data analysis determines the percentage of total variance for each factor. Two key effect sizes were considered:

- Partial eta squared: $\eta^2_p = SS_{effect} / SS_{effect} + SS_{error}$

challenging to clean. The key factors were standoff gap and component pitch.

The solder paste flux residue was also a significant factor. The water soluble solder paste was easier to clean but when flux

- Partial omega squared: $w^2_p = df_{effect}$ x $(MS_{effect} – MS_{error})/df_{effect}$ x $MS_{effect} + (N-df_{effect})$ x MS_{error}

For this study both were calculated and compared.

Table 13: Partial Eta Squared and Partial Omega Squared

Effect Size1-4	**Small Effect**	**Medium Effect**	**Large Effect**
Partial Eta Squared (η_p^2)	0.01	0.06	0.14
Partial Omega Squared (ω_p^2)	0.01	0.06	0.14

Partial Eta Squared analysis (Type 1) and Partial Omega Squared (Type II) finds that the Cleaning Method exhibits the highest level of significance. The factor of the greatest significance was the cleaning method that comprised either the Inline or Batch cleaning process. When cleaning leadless components, the cleaning fluid must penetrate, wet the residue, dissolve the residue, create a flow channel and fully remove all sources of residue. The inline process is equipped with spray jets that are perpendicular to the plane of the circuit board being cleaned. The energy from these spray jets create deflective energy to drive the cleaning agent to the source of the residue. The batch cleaning method delivers high flow but at lower impingement force. On low profile components, this cleaning method exhibited lower effectiveness. Other contributing factors were wash temperature, cleaning agent, wash time, and wash concentration.

The component being cleaned exhibited the second highest level of significance. The QFN and QFP160 components were the most residue from this paste was present, SIR values significantly declined. Water soluble flux residues must be completely cleaned. Partially cleaned No-Clean solder paste resulted in lower SIR values. There was little difference from the use of the Jet Printed solder paste versus the Stencil Printed solder paste.

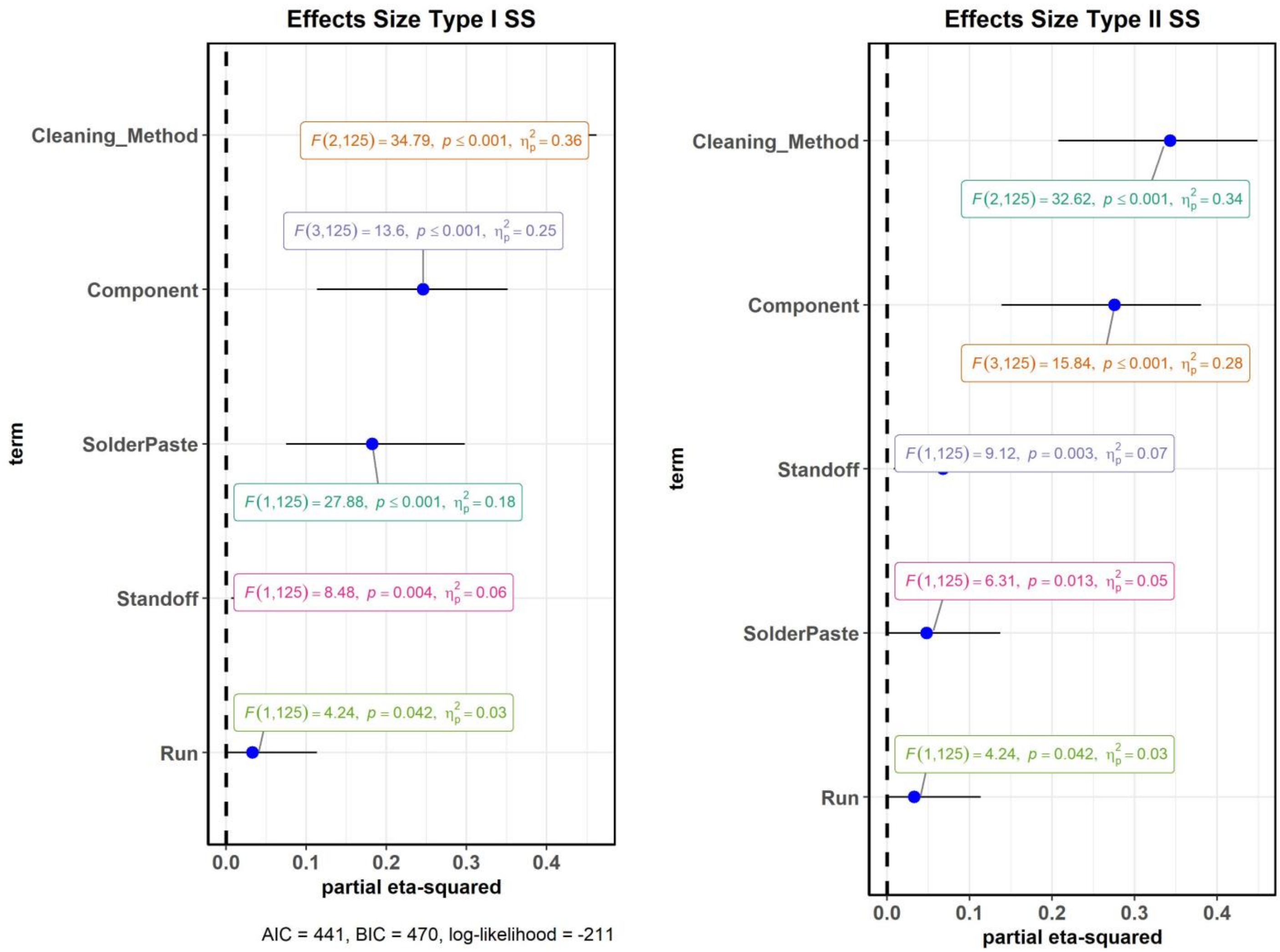

Figure 39: Type I and Type II Levels of Significance

Type II testing finds that the cleaning method and component type had the largest significant effect. Standoff, solder paste, and run (jet vs. stencil printing) had small effects.

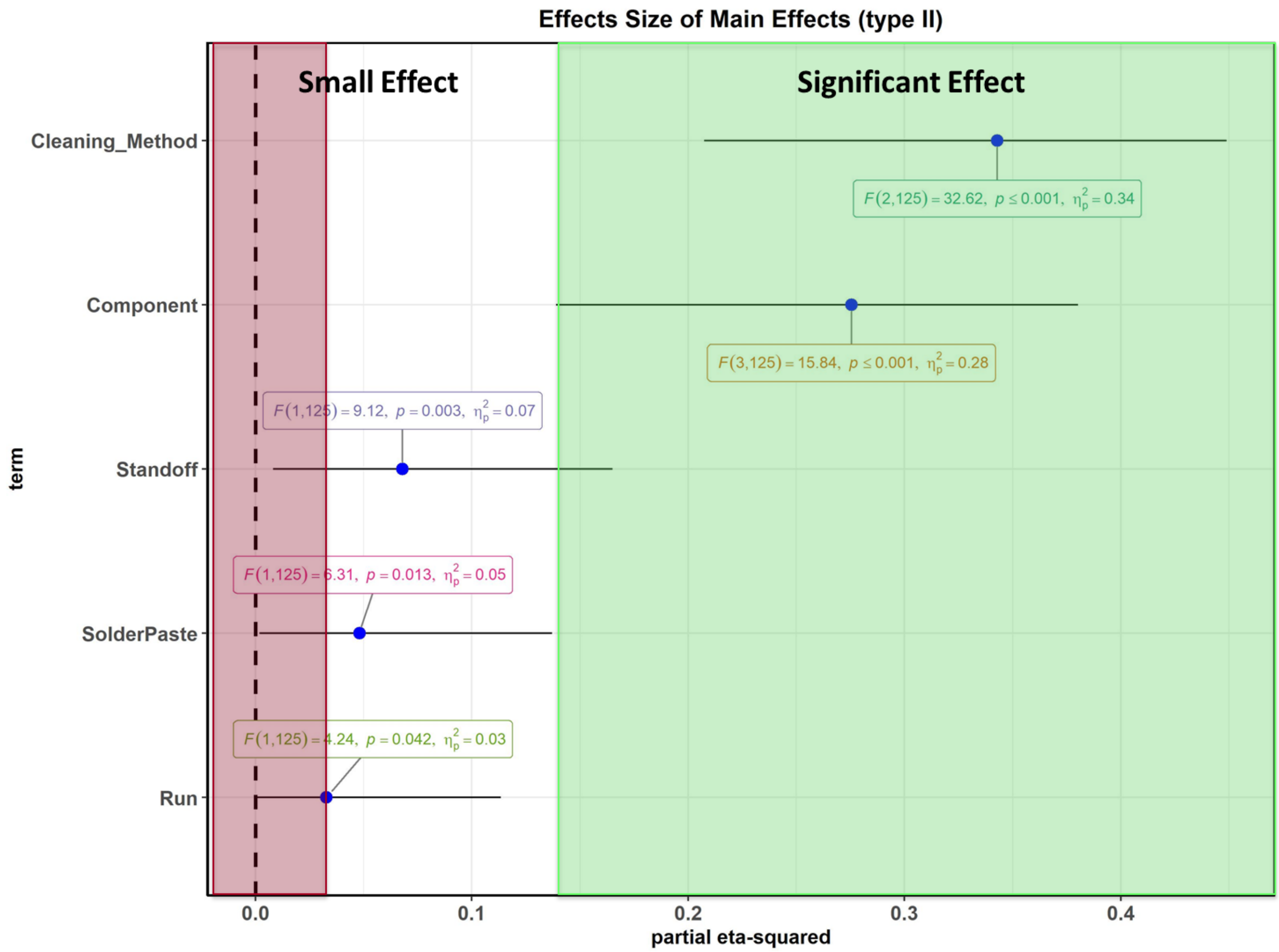

Figure 40: Type II Significant and Small Effects

The IC data analysis found slightly different results when compared to the SIR method. The factors of highest significance were the cleaning method, run (jet vs. stencil printed), solder paste and standoff. When performing the IC analysis, each quadrant was analyzed separately. This was done to reduce the understating of the IC values on sections of the board where no component was placed. The significant variables factored into the levels of anions and cations. For example, boards cleaned using the batch process resulted in higher levels of weak organic acids. The levels also varied for the jet printing versus the stencil printed boards. Both the solder paste and standoff gap influenced the levels of ionic contamination.

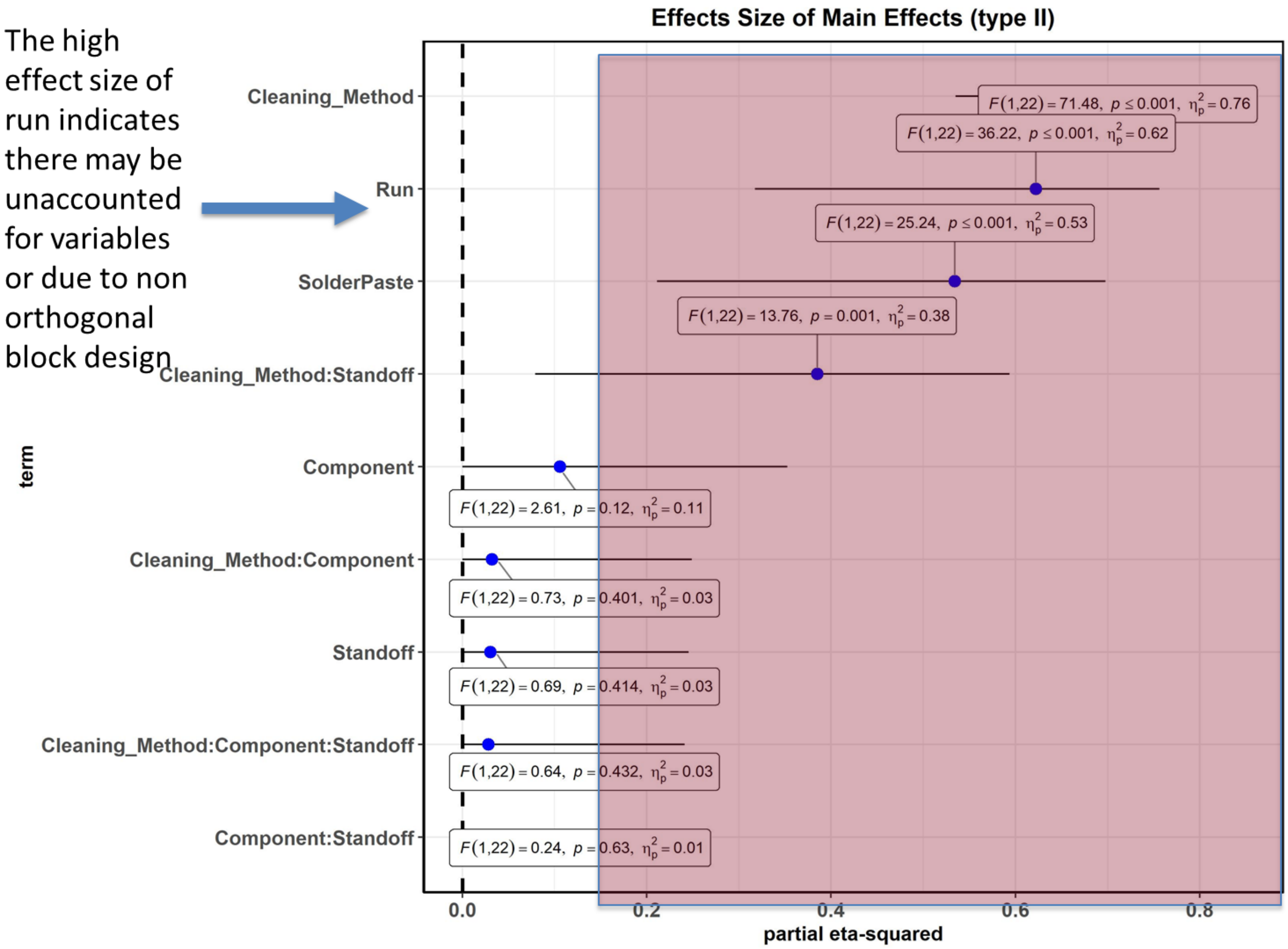

Figure 41: Ion Chromatography (IC) Levels of Significance

Failure Modes and Effecst Analysis (FEMA)

1. *Identify a failure mode* – The research finds that process contamination next to conductors and under the bottom termination lower surface insulation resistance due to metal migration in the form of leakage currents and dendritic growth. The data also finds that the problem is more pronounced based on the component design. Flux residues and other ionic residues left on a printed circuit board from the manufacturing process are a potential threat on specific component types.
2. *Identify the likely cause of failure* - No-Clean flux systems are designed to leave behind benign surface contaminants during wave and reflow soldering processes. As components miniaturize, higher I/O and tighter pitch narrow the conductive pathways under the components bottom termination. When there is a high termal mass of solder and low standoff gap, the soldering temperatures can vary in temperature due to block outgassing pathways. When this occurs, the activity of the flux residue can be active. These localized residues can cause electrochemical failures under the right conditions.
3. *Identify the failures probability of occurrence* – Components of the flux residue (most notably the weak organic acid activator system) in contact with water layer – formed due to humidity – can cause higher leakage current (reduction in surface insulation resistance (SIR)) between biased points on specific components. Active residues like carboxylic acids are hygroscopic and therefore influence the amount of water adsorption under humid conditions. Subsequent dissolution of the active part of the flux into the

adsorbed water layer then influences the SIR followed by detrimental electrochemical processes at the metallic connections.

4. Establish the likelihood of detection – Materials and Process Characterization / Qualification test methods are called out within industry standards. Both chemical and electrical test methods are performed to quantify any deleterious effects that might arise from solder flux or other process residues let on external surfaces after soldering, which can cause unwanted electro-chemcial reactions that grossly affect reliability. Test boards designed with critical components that are prone to trap flux residues and the use of SIR instrumentation can identify and analyze risks associated with contamination.
5. Identify and prove out corrective actions – Surface Insulation Resistance testing that can be done at the manufacturing site can be used to establish acceptable and unacceptable levels of residues on production hardware. Control measures such as SPC can be used to eliminate risk or mitigate their effects. This enables the process engineer to monitor changes to their process. The test method allows for printed circuit board design, process development, process control and product acceptance.

Follow on Research

The research completed provided a baseline on challenging components processed through the Inline and Batch process. Follow-on research will leverage the data findings from this research to develop design options and process conditions that demonstrate that a manufacturing process or process change that produce hardware with acceptable end-item performance related to electrochemical risk.

Once those conditions are defined, a Gage R&R study will be performed to gage repeatability and reproducibility of the cleaning process. From these studies, the plan is to measure the amount of cleanliness variation on defined test boards populated with problematic components. The goal will be to measure the variation in the cleaning process and the SIR test instrument.

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