DESIGNING A CLEANLINESS RISK PROFILE ON LEADLESS & NEAR CHIP SCALE PACKAGES

PRESENTED AT SMTAI 2020

ABSTRACT

The industry is moving toward leadless components with near chip-scale packages. The fastest-growing package types include leadless, passives, and a proliferation of new package styles that are larger with a higher number of connections. The advantages of these small components are well documented; however, concerns arise from the small overall dimensions, reliability, and manufacturability. Users must carefully select and validate whether these components are suitable in their intended use environments and customer applications. Soldering and cleanliness issues have been causal factors for many failures seen in production and the field.

For the electronics industry, predictive failure and end of life must be known. To increase the end of life and to have a predictive failure, it is imperative to understand the chemistry of materials. The activity of these materials at temperature and humidity can result in parasitic leakage and failure in challenging environments. The companies involved in designing, selling, and manufacturing the assemblies must mitigate potential failures by understanding these risks when developing and distributing the end product. The purpose of this research is to design a cleanliness risk profile using applicable test methods targeted on leadless and near chip-scale packages.

Keywords: Bottom Terminated Components, High-Density Interconnections, Designing for Reliability, Cleanliness, Electrochemical Failures, SIR

INTRODUCTION

IPC standards are used to guide the electronics manufacturing industry in producing acceptable electronic assemblies, components, and hardware. Printed wiring boards are classified based on expected life and reliability within use conditions. Four classifications were designed for the acceptability of electronics assemblies.[1]

Class 1 General Electronic Products: Class 1 boards represent general electronic boards with a limited life and a simple function. This class includes most typical everyday products. Class 1 boards allow for various cosmetic defects as long as it doesn't affect the functioning of the board.[1] Reliability is not a critical factor since the end product has a limited life expectancy.

Class 2 Dedicated Service Electronic Products: Class 2 boards have higher reliability and extended life. These boards follow more stringent standards than Class 1 but allow some cosmetic imperfections. Here, uninterrupted service is preferable, but not critical. Class 2 products aren't exposed to extreme environmental conditions.[1] The board is expected to run continuously, but its operation is not overly critical. Typical products include laptops, smartphones, tablets, communication equipment, etc.

Class 3 High-Performance Electronic Products: Class 3 boards must provide a continued performance or performance on demand. There can be no equipment downtime, and the end-use environment may be exceptionally harsh. High levels of inspection and testing are performed on these boards with stringent standards. This makes the class 3 boards highly reliable.[1] This category includes critical systems such as life support systems, military equipment, electronic monitoring systems, automotive, etc.

Class 3/A Space and Military Avionics: IPC 6012 is a new class that represents the highest class for printed circuits. The class 3/A boards call for very stringent manufacturing criteria since the boards should remain operational in critical conditions, such as the International Space Station. Class 3/A boards are expensive to manufacture compared to the other classes since they need to be close to perfection.[1] They are found in aerospace, military airborne systems, and missile systems.

ELECTROCHEMICAL FAILURES

Electronic assembly designs increase in complexity as customers demand more features with higher clock speeds. As the electronics industry changes to meet these demands, circuit cards have higher wiring density per unit area as opposed to conventional

circuit boards. These highly dense boards incorporate finer spaces and lines, small vias, and higher connection density.

No-clean flux has become the predominant flux used in electronic PCB assembly. No-clean fluxes are designed to leave low residues that are non-conductive. If appropriately used, no-clean flux can be effective, safe, and reliable.[2] To build these highly dense assemblies, the use of leadless and bottom terminated components evolved. These small bottom terminated components were found to trap heavy flux residues under the component terminations. As a result, the electronics industry is experiencing a greater number of product recalls, product returns with no defects found, and hard short failures due to electrochemical migration.[2]

Three critical factors require consideration and assessment.

1. Standoff gap
   a. Lower standoff gaps block outgassing channels
   b. Flux activators and functional additives within the flux package may not decompose per specifications
   c. Active residues are at a higher risk of electrochemical migration
2. Narrow Pitch
   a. The decreased distance between conductors
   b. Large pad dimensions decrease pitch
   c. Higher risk for bridging conductors with flux residue
   d. Electrical field increases
3. Cubic Volume of Flux
   a. Increased I/O result in Pitch and Pad Dimension variations
   b. Higher volumes of flux result under the bottom termination since both functional additives and activators do not properly outgas
   c. Active and pliable flux has a greater potential for electro-migration through flux residue

Electrochemical reliability is not constant across the circuit card. Failure potential is often site-specific. High-risk areas include materials selection, component types, multiple soldering steps, selective soldering, wave soldering, rework, cleaning, and coating. To illustrate, the test board shown in Figure 1 is a 4-channel SIR test board. Channel 1 is populated with the QFN-48 component. Channel 2 is a 244 I/O BGA with a center lug. Channel 3 is a QFP-160 laminate dummy with an SIR comb pattern. Channel 4 is an array of caps ranging from 0201, 0402, 0603, and 0805. Notice in Figure 2 how the insulation resistance values vary based on the component type. When designing a risk profile, the focus should be centered on materials characterization, reflow, number of soldering steps, component types, and when cleaning is required – the process conditions to validate the process.

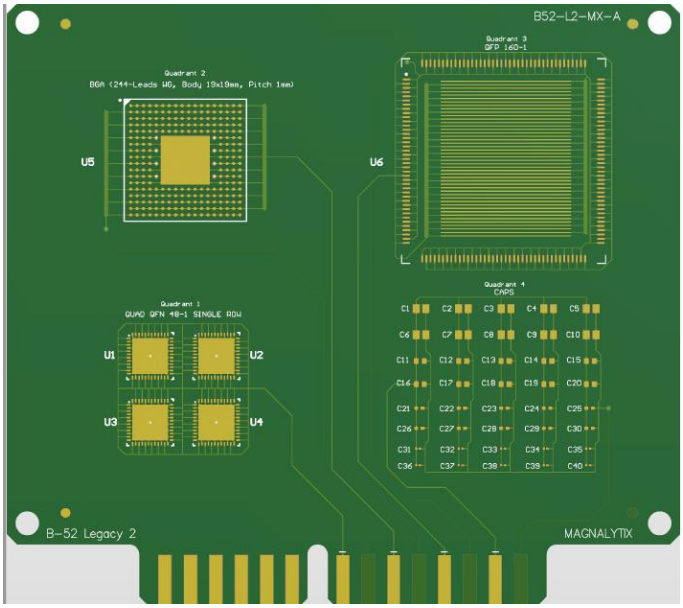

Figure 1: *4-Channel SIR Test Board*

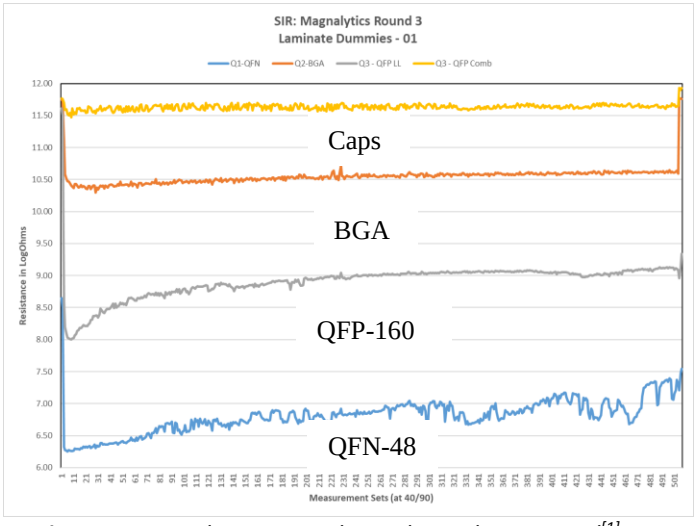

Figure 2: *SIR Values across the 4-Channel Test Board*[1]

CLEANLINESS RISK PROFILE

Failures that occur in the field consume valuable engineering time and resources to perform failure analysis. Focusing on problems after they occur is a reactive approach that consumes valuable resources

that could be better used to grow the enterprise.[4] The purpose of this research paper is to develop a proactive methodology to determine electrochemical reliability using highly accelerated life testing.

All manufacturing processes result in process residues on circuit assemblies in one form or another. The challenge many assemblers battle is variation as part of daily manufacturing. Problematic process residues may not be detected using standard inspection methods. Test methods using temperature, humidity, and bias effectively detect residues that could cause a reliability issue.

IPC J-STD-001H – Section 8.1 defines a "Qualified Manufacturing Process." *Unless otherwise specified by the User, the Manufacturer shall [N1D2D3] qualify soldering and/or cleaning processes that result in acceptable levels of flux and other residues.*[5]

The methodology for "Designing a Cleanliness Risk Profile" focuses on the following:

1. Component Considerations
2. Printed Circuit Board
3. Materials Characterization
4. Assembly
5. Rework

STEP 1: Component Considerations

Designing for cleanliness reliability is hardware-specific. The risk factors are most prominent for Class 3 and Class 3/A products. As such, OEMs go to great lengths to understand risk potential and to design their hardware to mitigate those risks. Process contamination is one of the potential risk areas.

Circuit cards with more components tightly placed increases the opportunity for process contamination. As components reduce in size, reductions in package height, standoff, and pitch can leave pockets of contamination across conductors of opposite polarity. If these process residues are not properly outgassed, the residue pool can be active. If operated with a harsh environment, where atmospheric moisture is present, there is potential to develop leakage currents which can lead to intermittent device failures.

Figure 3 illustrates the residue pool under a BTC on an SIR glass test board following soldering. Notice the levels of flux next to signal pins and from the ground lug to the signal pins: the residue bridges conductors or opposite polarity. If the flux was not correctly outgassed, resistance against metal migration would not be achievable.

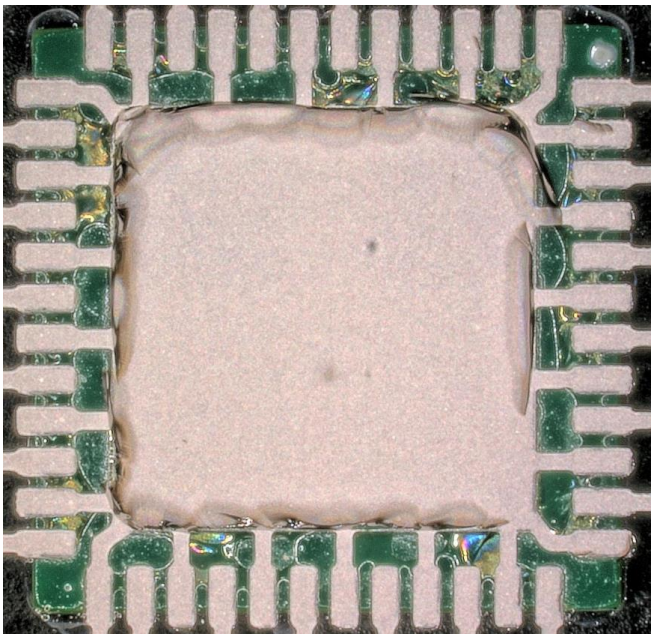

Figure 3: *Process Residue under Bottom Termination*

Across a circuit board design, components whose external connections that consist of planar metalized terminations pose some of the highest risks for trapping process residues. Since the pitch and standoff heights are incredibly tight, these components are valuable for characterizing contamination risks.

Designing SIR test boards that allow for temperature-humidity-bias testing using components that exhibit the highest risk potential enables critical intelligence during the design and qualification. Figure 4 illustrates a test board design for understanding electrochemical interaction risks on some of the most challenging components used on a particular board design. The data gained from this type of testing allows the assembler to select the best materials and process conditions that achieve electrochemical reliability. By isolating the weaknesses early in the design process, engineers can prove their process conditions.

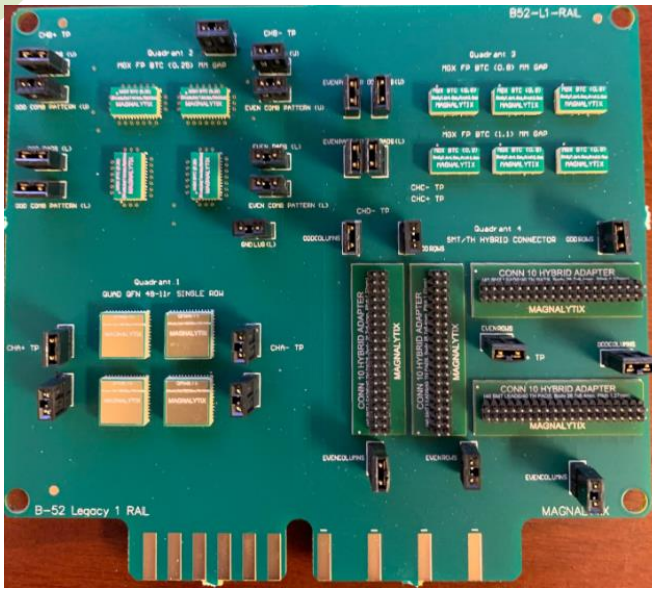

Figure 4: *Custom Test Board Design*

STEP 2: Printed Circuit Board

Solder mask is a polymer applied over copper traces on the printed circuit board for protection against oxidation and to prevent solder bridges from forming between closely spaced solder pads. The solder pads can be defined with the solder mask, non-defined, or no-solder mask defined from pad to pad. Removal of the solder mask aids in flux outgassing. This approach can significantly reduce the levels of flux residue under the component termination.

Solder Mask Defined (SMD) is to define the pad area with solder mask. Solder mask defined pads are suitable for fine pitch components.[6] The solder mask is patterned to the pads, typically overlapping on the pad edges. The advantage of solder mask defined pads is the reduction of pad lifting and bridging. The disadvantage, standoff gaps are reduced, which allows flux residue to fill all cavities under the component.

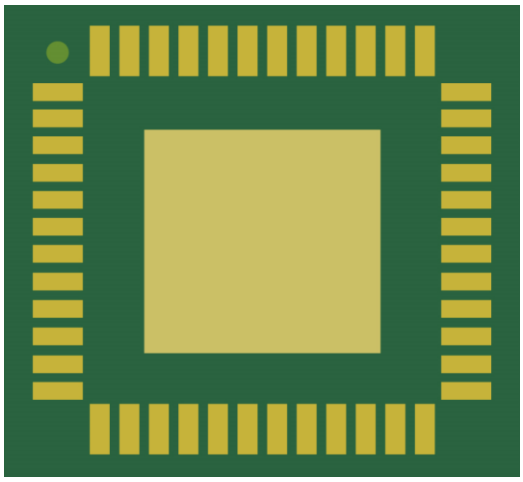

Figure 5: *Solder Mask Defined (SMD) Pads*

Non-Solder Mask Defined pads differ from SMD pads as the solder mask is defined not to make contact with the copper pad.[7] Instead, the mask is patterned to create a gap between the edge of the pad and the solder mask. Removal of the solder mask defining the copper pad allows for wider trace widths. The advantage is that the flux residues have a narrow channel to outgas, which reduces flux residue bridging the signal pins.

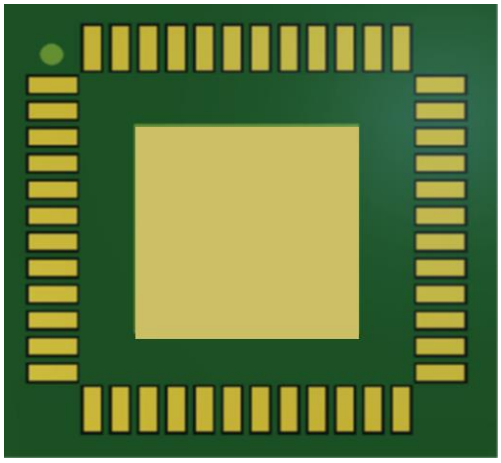

Figure 6: *Non-Solder Mask Defined Pads*

For fine-pitch devices (e.g., 0.4mm pitch), it may not be possible to maintain a solder-resist dam between neighboring I/O copper pads due to the minimum thickness of the solder mask dam.[8] Solder mask dams typically require a minimum width of 0.150mm to ensure robust solder mask adherence. A ganged solder mask design removes all solder mask in the pad area. The disadvantage is a more significant potential for solder bridging. The advantage is better clearance for

flux outgassing and lower levels of trapped flux residues under the component termination.

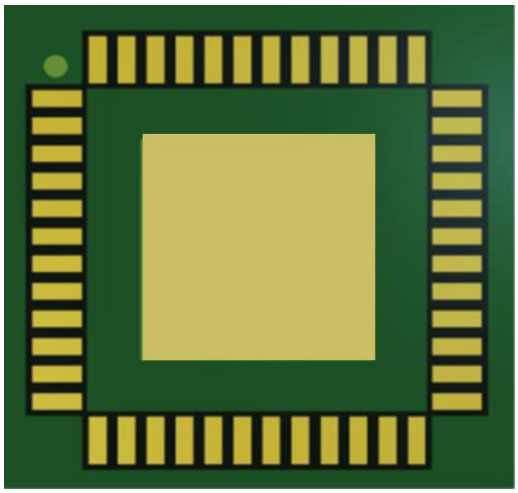

Figure 7: *Ganged Pads – Removal of Solder Mask*

A characteristic of BTC packages is the inclusion of a solderable thermal lug found on the underside of the component. The thermal lug is positioned directly under the silicon die within the package. The thermal lug helps to dissipate heat from the component to the inner layer PCB ground plane. Since the thermal lug is a reflowed solder pad, during reflow, flux residues push away from the thermal lug onto the solder mask areas surrounding the thermal lug. The flux residue can bridge the thermal lug to the signal pins. The flux residue can cause electrochemical failures due to poor outgassing and the sheer cubic volume of flux.

On some designs, thermal vias are patterned within the thermal lug to aid in dissipating heat. These thermal vias can also help in flux outgassing.

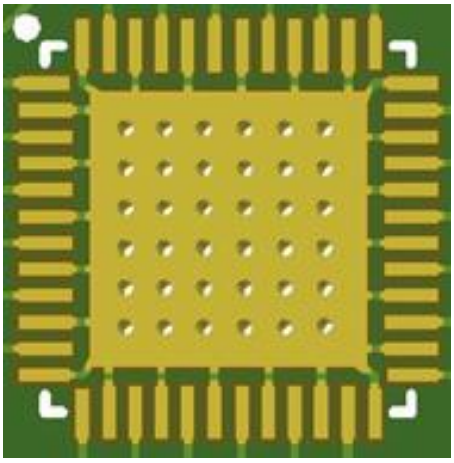

Figure 8: *Thermal Vias patterned into the Ground Lug*

Solder Mask Windows that are patterned within the Thermal Lug has been found beneficial for both heat dissipation and flux outgassing. A secondary benefit is a void reduction within the thermal lug itself.

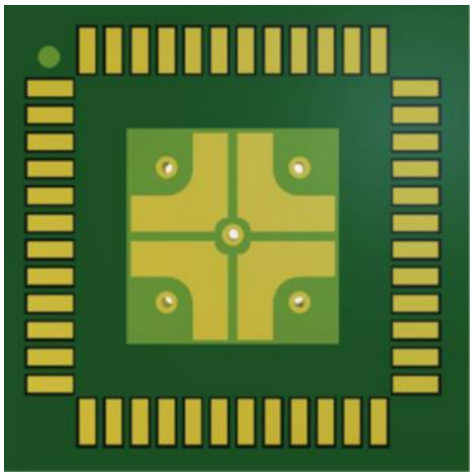

Figure 9: *Solder Mask Windows + Encroached Vias*

In summary, leadless and bottom terminated components trap process residues under the component termination. Both pitch reduction and lower standoffs inhibit flux outgassing. Factoring in printed circuit board design features that provide channels to outgas flux residues will improve electrochemical reliability. These features reduce the cubic volume of flux under the component termination, which aids in removing all process residues during the cleaning process.

To illustrate, the test board in Figure 10 was designed to determine the best pad design for rending the highest electrochemical reliability on a No-Clean design.

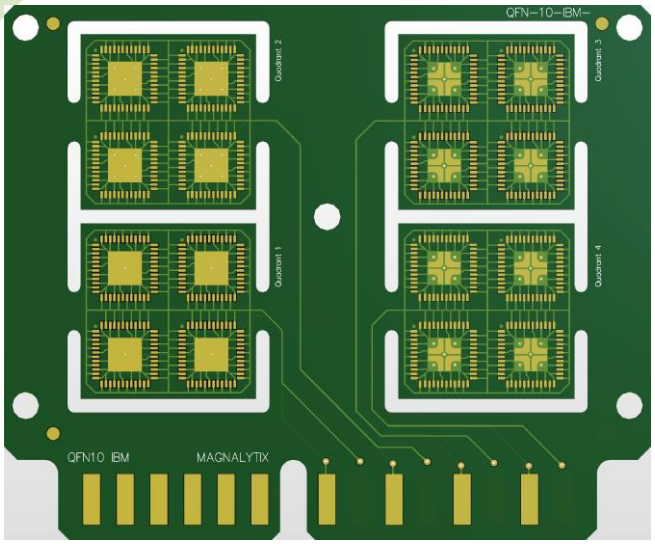

Figure 10: *Custom Test Board to Study Flux Outgassing*

Quadrant Test Parameters

- Quadrant 1
  - Open Copper
  - Singulated I/O
  - 8 mil thermal vias placed into the thermal pad
- Quadrant 2
  - Open Copper
  - Ganged I/O
  - 8 mil thermal vias placed into the thermal pad
- Quadrant 3
  - SMD Thermal Pads
  - Ganged I/O
  - Encroached Vias
  - 8 mil thermal vias within a solder mask web
- Quadrant 4
  - SMD Thermal Pads
  - Singulated I/O
  - Encroached Vias
  - 8 mil thermal vias within a solder mask web

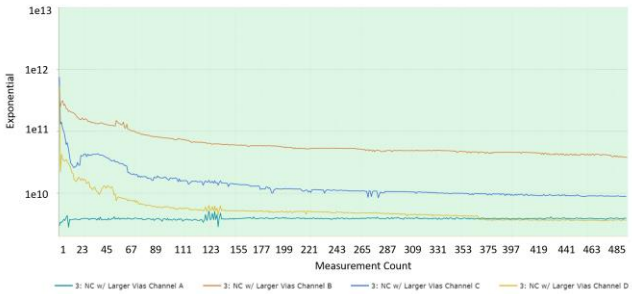

Figure 11*: SIR [40/90 – 168 Hours – 5v Bias]*

Quadrant 1 and 4 patterned with singulated signal pins had lower SIR values. Quadrant 2 with ganged signal pins and thermal vias in the ground lug had the highest SIR value. Designing test boards that allow the designer to characterize materials and their effects when exposed to harsh conditions enable them to reduce risk and improve reliability.

Step 3: Materials Characterization

The assembly of electronic modules, printed circuit boards, and sub-assemblies encompass numerous materials. These materials all result in the formation of process residues. Many of the components used to build electronics are cleaned. Whether the final assembly is designed as a "No-Clean" or cleaned, the characterization of materials is a critical step to understanding the cleanliness risk profile.

Highly dense assemblies require smaller via structures. As PCB board layers increase and become more complex, there is the risk of metallic filament formation within the printed circuit board known as "CAF." CAF formation is a process involving the transport of conductive chemistries across a non-metallic substrate under the influence of an applied electric field.[9]

CAF commonly occurs between adjacent vias (i.e., plated thru-holes) inside a PCB.[10] As the copper migrates along with the glass/resin interface from the anode to the cathode, CAF failures can manifest as current leakage, intermittent electrical shorts, and even dielectric breakdown between conductors in printed circuit boards. This often makes CAF very difficult to detect, primarily when it occurs as an intermittent issue. SIR custom test boards or break-off coupons patterned in waste areas within the panel design can be used to characterize the plating and bare board cleanliness.[11] The test can also be used to monitor incoming board cleanliness. Figure 12 illustrates a custom test board for the characterization and cleanliness of the incoming PCB.

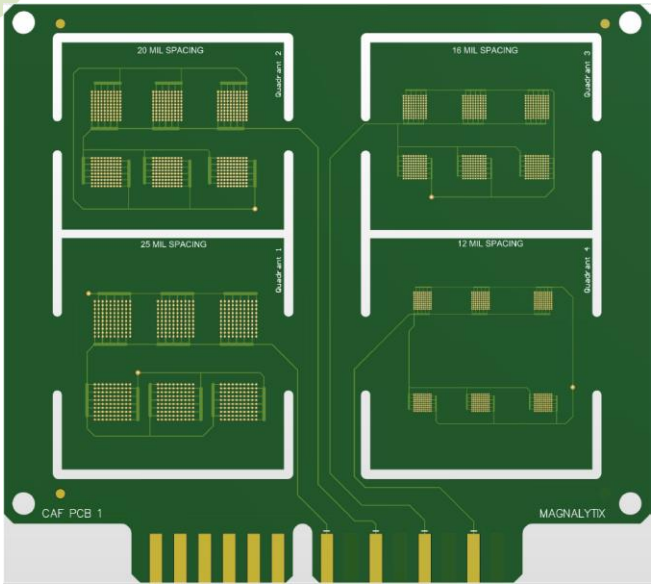

Figure 12: *Custom Test Board for CAF and Board Cleanliness*

Soldering processes used to mount the components to the Printed Circuit Card involves numerous materials that must be carefully selected to reduce risk and ensure reliability. The heart of soldering is wetting. The metallurgical bond occurs only in the presence of clean surfaces.[12] Once wetting occurs, an intermetallic compound forms.

Solder pastes and alloys require "flux" to improve wetting and solderability. Flux is a chemically active compound that, when heated, removes surface oxidation. Flux contains oxygen barriers to prevent reoxidation of the metals being soldered. Flux promotes the formation of an intermetallic layer between solder and metal.[12]

IPC J-STD-004B designated flux types and the activity of the flux. Figure 13 lists the common flux types.[13]

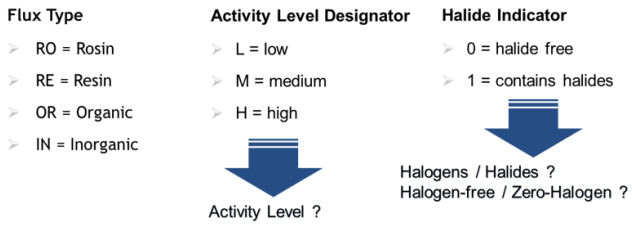

Figure 13: *Flux Types*

Common flux types include:

- No-Clean
  - Low Residue
  - Encapsulates metal oxides in a rosin/resin hydrophobic barrier
  - Activators are typically weak organic acids designed to decompose during reflow
  - Non-conductive
- Rosin Mildly Activated
  - Leaves a rosin residue – partially hydroscopic
  - Softens at 60-70°C
  - Activators may be present in residue
  - Typically cleaned
- Organic Acid (Water-Soluble)
  - Flux components are soluble in water
  - Activators are strong and active
  - Generally very corrosive
  - Cleaning is mandatory

Flux selection depends on the application. This encompasses the product type, surfaces to be soldered, solderability of the component, and flux application method.[12] The activators used in the flux are ionic in nature. They are needed to remove metal oxides. They are heated activated and consumed during the reflow profile.

Surface Insulation Resistance (SIR) test method is used for incoming inspection, materials investigations and qualifications, quality conformance, prediction of long-term failure mechanisms, and as a predictive tool for estimated service life.[14] Electrochemical reactions at or below the surface of electronic circuits will affect their SIR.

SIR is performed in the presence of temperature, humidity, and electrical bias. SIR is considered the "gold standard" for characterization of process chemistries, which include solder masks, solder paste residues, wave soldering residues, selective, manual soldering, and rework. SIR is also effective at testing the moisture barrier of conformal coatings.[14]

Temperature-Humidity-Bias tests are used to test for electrochemical migration or electrochemical corrosion. The temperature and humidity tests artificially age a materials system. This highly accelerated test regime can simulate years of service by days of testing. The test is effective at developing a risk profile of service life.

Temperature-Humidity-Bias testing detects evidence of the loss of integrity or reliability in a materials system. Loss of integrity may include conformal coating or solder mask adhesion failure, decreases in

dielectric strength, electroylic corrosion, or electrochemical migration.[14] Each of these may represent shortcomings in materials, manufacturing methods, ore a susceptibility to a particular failure mechanism.

To illustrate, the IPC-B-24 test board can be used to evaluate the activity of soldering materials. IPC TM-650 2.6.3.3 test method calls for the B-24 test board to characterize fluxes that determines the degradation of electrical insulation resistance of rigid printed wiring board specimens after exposure to the flux system.[15] The B-24 test board is illustrated in Figure 14. The open comb test pattern is used to test the activity of flux residues after heat activation through the soldering process.

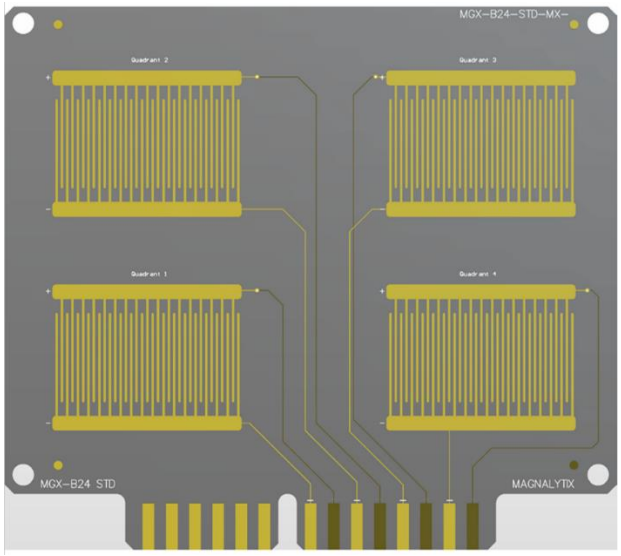

Figure 14: *IPC B-24 Test Board Design*

Figure 15 is a chart of the SIR insulation resistance from a No-Clean Solder Paste evaluation. All four channels of insulation resistance exceeded 10 $Log_{10}\Omega$s and were stable over the test period.

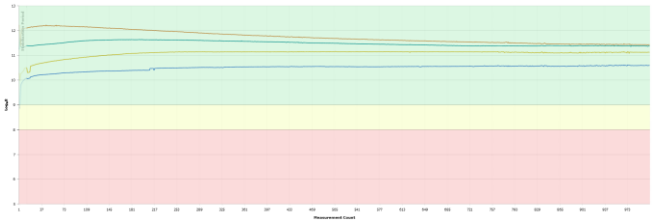

Figure 15: *Solder Paste SIR test using the B-24 test board*

STEP 4: Assembly

During assembly, it is critical to qualify and control the assembly for cleanliness. SIR was initially designed to characterize soldering materials. As previously stated, open comb test boards are used for classifying the flux component. Solder paste and other soldering materials develop their products to the open comb patterns.

Small leadless and bottom terminated components can trap flux activators and other functional additives under the component termination. Activation temperature, activation time, reflow profile, and component density can change the properties of the remaining flux residue.

In or around 2001, IPC introduced the IPC-B52 SIR Test Board. The B-52 SIR test board includes test patterns adjacent to, and beneath, several components.[14] Components were chosen to represent typical constructions and spacings during that time. The intention was a design that measures insulation resistance across the components conductors of opposite polarity. On components that entrap process materials, SIR has been shown to be effective at detecting partially cleaned residues.

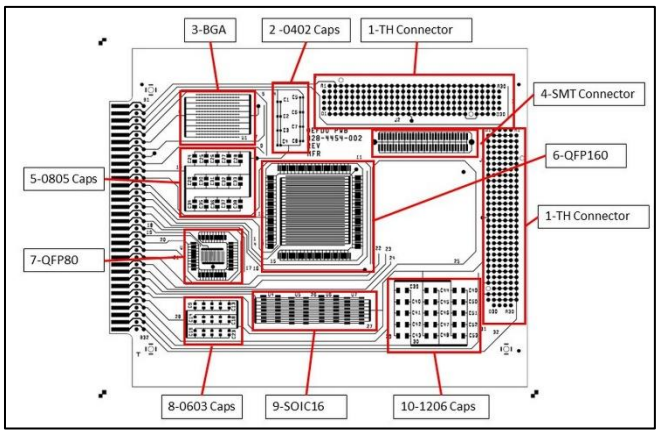

Figure 16: *IPC B-52 SIR Test Board*

If you are building your assemblies to a “No-Clean” standard, controlling all incoming materials and the final assembly for cleanliness is critical. No-Clean is a mindset. Incoming parts must meet defined cleanliness standards. Surface insulation resistance is highly effective for reducing risk by characterizing solder pastes, wave fluxes, selective soldering, and rework.

If you are cleaning your assemblies, characterizing wash chemistries, cleaning machines, process conditions, and rinsing are vital factors. On highly dense leadless and bottom terminated components,

poor cleaning and rinsing can impact reliability. Custom SIR test boards that are representative of the most challenging component types on production hardware allow an assembler to dial in the process conditions to meet the design objective. SIR is highly effective at determining “how clean is clean enough.”

The IPC Cleanliness Spec allows companies the use of a custom-designed SIR test card that replicates their actual hardware, and that is agreed upon by the manufacturer and user. This allows the manufacturer and user to develop real solutions that are tailored to their unique electronic component and manufacturing challenges, and end-use environments to gather objective data at their site-specific locations and correlate it to their actual hardware.

Custom SIR test boards can be engineered to meet the most challenging component problems. Some designs are populated with components that entrap wash fluids. The key is to build-in design points into the test board that causes field problems. Making an accurate data set to study the problem helps an OEM develop and test solutions that resolve the issue.

Figure 17 illustrates a test board designed with BTCs, SMT connectors, and SMT/Thru-hole connectors. The objective is to give the OEM or CM confidence that their reflow profile is achieving proper outgassing of the flux residues if they are running a “No-Clean” process. If the assembler cleans, this test board is effective at evaluating SMT and Wave/Selective soldering processes.

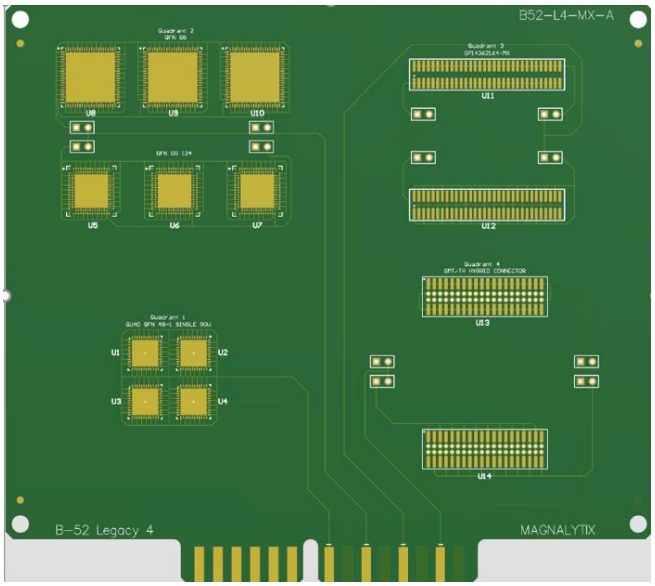

Figure 17: *Custom SIR Test Board Design*

A second example is the use of test coupons employing SIR test patterns as a process control plan. The coupons are representative of materials and components that are representative of actual electronic products/hardware. The assembler can use these SIR test coupons as part of the procedure to qualify the manufacturing process.

The SIR results for these test coupons are then used to establish control limits above and below the actual SIR data that is defined in the qualification units and process. This data becomes a baseline SIR test to measure future builds on a lot to lot basis. This Baseline SIR data is developed by running a statistical sample size of test boards through a 40C/90% RH or 85C/85%RH temperature/humidity environmental test plan using a damp heat chamber / controlled humidity chamber for 168-hours to qualify the process and collect objective evidence to J-STD-001G. SECTION 8 specification.

Figure 18 is an example of four test coupons that can be patterned into the panel of production boards. The test coupons are populated simultaneously with the production boards.

This test coupons are then run periodically as the process control test vehicle to correlate the data to the qualification units – Baseline SIR data that was initially run to verify and validate the material choices and process parameters. The test coupon is tested using SIR, with acceptable upper / lower limits that is agreed

upon between the manufacturer and their customer, and this allows one to use a process control technique to monitor future builds to the initial qualified "baseline" units that were correlated to actual electronic hardware.

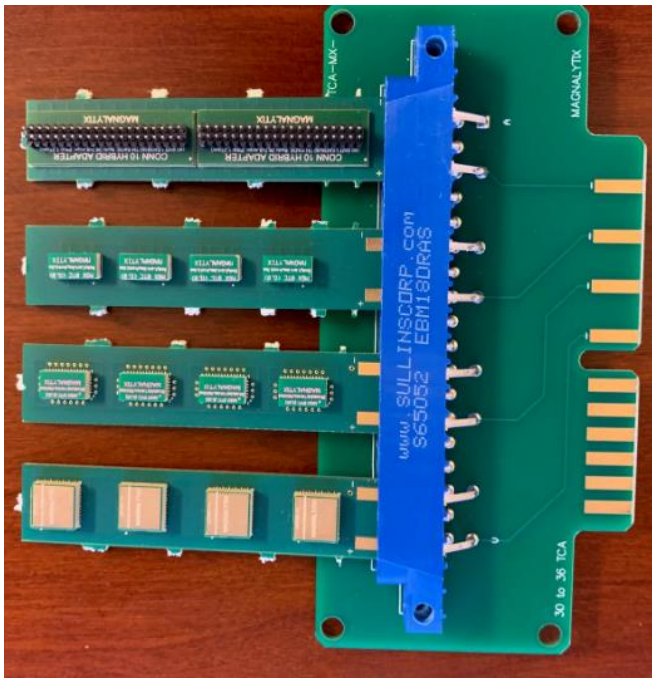

Figure 18: *Process Control SIR Test Panels*

This process control technique can then be used at some predetermined frequency to ensure the correlation between the qualification build and future production builds to determine any drift in actual output as it relates to manufacturing processes or process materials.

STEP 5: Selective Soldering/Rework

Selective Soldering

Selective soldering applications pose unique problems due to the localization of the soldering process. The process requires high precision, especially when running a No-Clean process. Flux deposition on the board must be carefully controlled.[16] The physical characteristics of the flux combined with selective soldering equipment are mandatory to achieve both solderability and reliability.

Wave solder liquid fluxes are designed to wet and spread. The risk of using a wave solder liquid flux with excellent wetting properties is the movement of the flux to other neighboring components. During the selective soldering process, unactivated flux left in areas outside the soldering point could cause reliability issues in the form of leakage currents and dendritic growth. The process of building reliable assemblies centers on the flux, process parameters, selective soldering machine, and material properties.

Localization of the flux residues through a drop jet fluxing process is not enough to guarantee the expected performance level. The flux design must be engineered to minimize the impact of unavoidable spreading and satellite events. These events will result in partially heated flux residues, which won't be removed by the washing action of the solder.[17] They pose a severe threat to the reliability of the assembly, as ionic residues can induce electrochemical migration, corrosion, and resistance losses, which will invariably result in in-field product failures.

The fluxer configuration on the selective soldering machine plays an integral part in applying the flux, controlling the preheat profile, maintaining heat to the soldering alloy, and soldering each filet without the formation of solder bridges. The flux must work in concert with the drop jet dispensing head to flow seamlessly during the entire operation, localize the deposit and finally stay in place.[17] The fluxing process parameters (Open time, Frequency, Robot Speed), as well as the board, preheat temperature are critical parameters, and their optimal settings depend upon the characteristics of the flux (viscosity, surface tension, solid content, solvent).

Fluxes and flux residues have often been identified as the root cause of electrochemical failures. Flux chemistry is becoming increasingly complex, and so even changing fluxes within one J-STD-004 flux classification (e.g., going from one ROL0 flux to another ROL0 flux) will result in a different residue assay. Since an electronic assembly represents a sum of residues from the process, flux residues from the SMT process may interact with flux residues from the selective soldering process. To illustrate this point, Figure 19 shows the spread of flux jetted onto litmus paper. It is critical that the flux not spread during application, especially when running a No-Clean process.

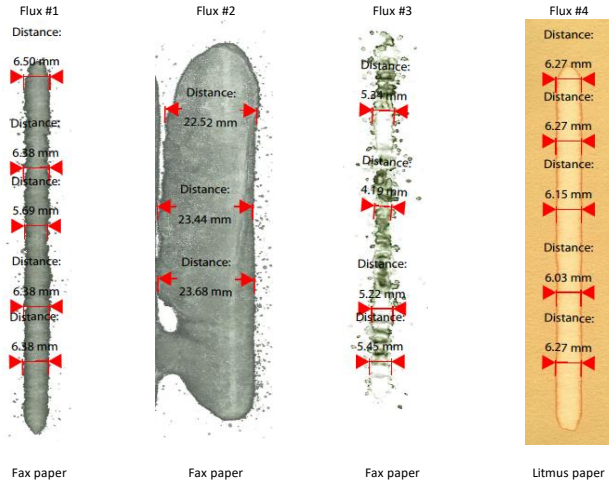

Figure 19: *Selective Solder Flux Spreading*

Several factors needed to achieve a reliable process:

- Soldering equipment
- Profile settings
- Flux composition
- Application of flux
- Solder temperature

Fluxing parameters:

- Open time
- Frequency
- Robot speed

Optimizing the selective soldering equipment and selection of the flux is critical to success. On highly dense leads, speed must be optimized to prevent bridging.

Figure 20: *Optimizing the Process Settings*

A double-sided SIR test board is ideal for optimizing both selective soldering and rework. The test board has 1206 caps on the top and bottom sides of the board. The connector has both SMT and fine pitch leads.

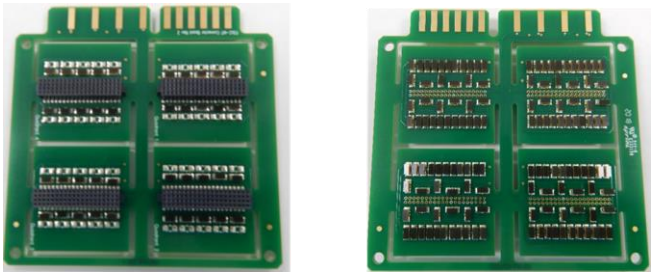

Figure 21: *SIR Test Board for Process Characterization*

To illustrate the variability in flux materials, Figure 22 shows the SIR results from the characterization and selection of the best flux chemistry. The boards were not cleaned following the selective soldering process.

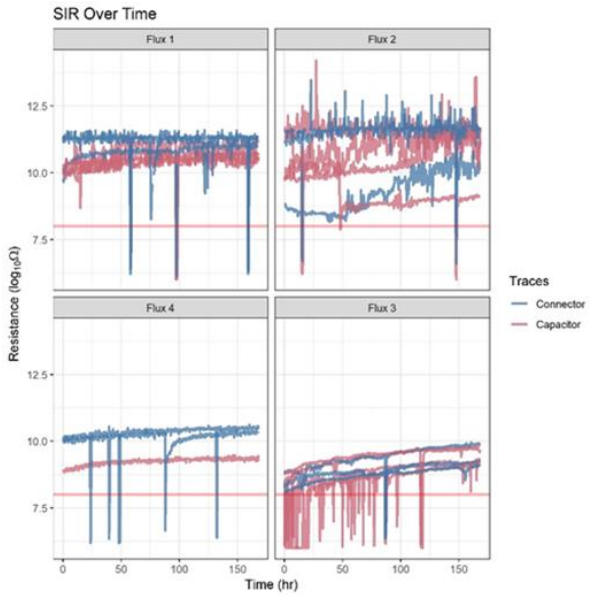

Figure 22: *Flux Characterization Testing using SIR*

Flux that wets to adjacent components does not experience the proper heat activation. When this occurs, there is a high risk of parasitic leakage. The downward spikes in Figure 22 is a direct result of this problem.

Rework

Rework is similar to selective soldering in that flux is needed to remove, clean, and replace the required component. When reworking a part, the use of a rework station is best practice. Solder stations help the operator control and monitor temperature profiles. Precision cameras enable accurate position. Temperature sensors prevent thermal overload.

Process contamination from handling can create solderability issues. Controlling contamination from the repair is critical. The prevention of contamination

sources from handling is equally important. A guide to benchtop PCB rework and repair is useful in understanding the best rework and repair methods.[18]

There are several procedures that can introduce contamination during the rework process. First, during desoldering, the use of solder wick, solder suckers, and heat are needed. The solder wick is coated with rosin flux to aid in the removal of the part. Proper cleaning and preparation before placing and soldering the new component is best practice. After the rework and replacement part is completed, cleaning is often necessary.

Topical cleaning is commonly used to remove the flux residues from the reworked area. During the cleaning step, there is a risk of the cleaning agent and soil spreading to other components in the areas where the cleaning occurred. As such, the cleaning step can add contamination to the area, which can cause electrochemical failures once the part is placed in service. Qualifying and validating the rework process is needed to understand this area of a cleanliness risk profile.

SIR testing is a valuable tool for training and qualifying the rework process. The test board in Figure 23 is useful for developing your rework methods. After the part has been removed, the use of a wire core solder with flux added is best practice. The use of a 0.015" diameter solder wire, using a P3 ratio is recommended.

Figure 24 & 25 is an example of SIR data that is helpful in developing the rework process. Figure 24 shows a rework process where cleanliness was a concern. Figure 25 shows a rework process where cleanliness was in control.

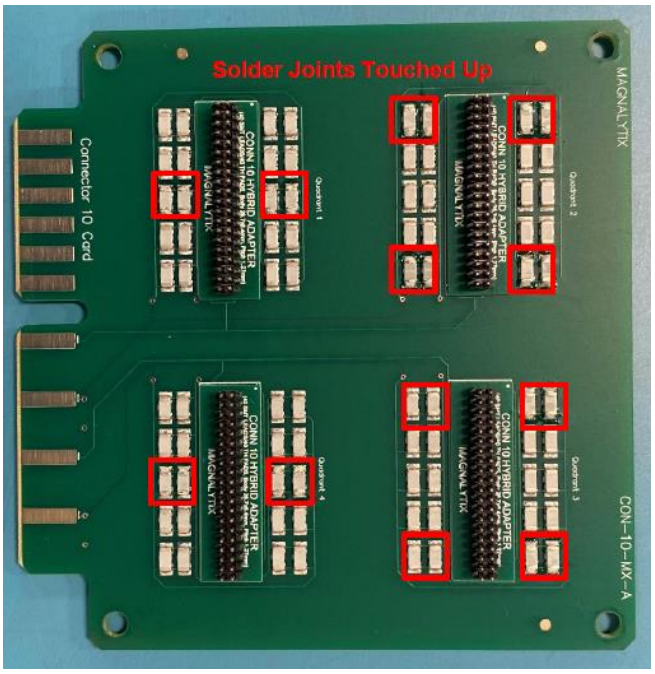

Figure 23: *SIR Test Board for Qualifying the Rework Process*

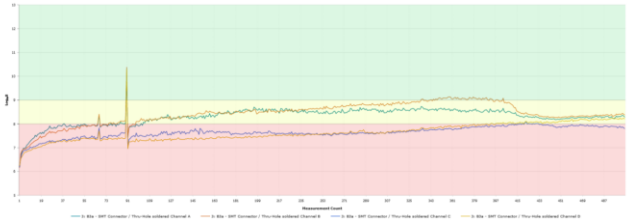

Figure 24: *Rework Cleanliness not Adequate*

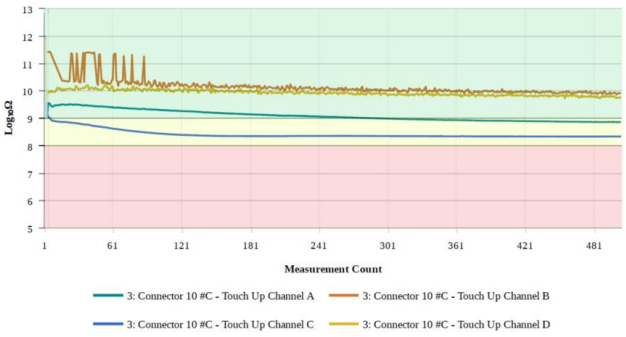

Figure 25: *Rework Cleaning in Control*

CLEANLINESS RISK PROFILE

All manufacturing processes result in process residues on circuit assemblies in one form or another. The challenge many assemblers battle is variation as part of daily manufacturing. Problematic process residues may not be detected using standard inspection methods.

Designing a Cleanliness Risk Profile focused on:

1. Component Considerations

2. Printed Circuit Board
3. Materials Characterization
4. Assembly
5. Rework

SIR test methods using custom test boards enable the OEM and CM to study component and design consideration, characterize materials, optimize the assembly process, control the assembly process, and characterize both selective soldering and rework.

SIR has long been known at the gold standard. Electronics Reliability Testing labs commonly performed this test procedure. The test was focused on qualifying the process itself. Utilizing this test method at the assembly site was not common. Advances in software, system integration, and test boards allow this powerful method to become a tool at the assembly sites. The use of this tool enables both the OEM and CM to develop a cleanliness risk profile across the many processes used to produce production hardware.

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