PROCESS CONTROL PLAN TO MONITOR ACCEPTABLE LEVELS OF FLUX AND OTHER RESIDUES

PRESENTED AT SMTAI 2020

ABSTRACT

IPC J-STD –001G, Amendment 1 requires that the assembler have a sampling plan to assure that the process remains in control once qualified and validated. It is well documented that electrochemical failures occur at component sites where flux residues are not fully activated. It is also well known that specific components have a higher risk of electrochemical failure. Selecting a control plan that monitors the process and its performance on challenging components provides assurance that the process maintains control once established during process qualification.

The test board used to qualify the process establishes an upper and lower spec limit for each of the component types on the test board. Surface Insulation Resistance upper and lower control limits, using challenging components that are representative of production hardware, represent a golden process condition. The golden image is a measure of process deviations that represents the performance of a resistance curve within a specific period. The objective is to judge whether the process in or out of control.

Keywords: Electrochemical Reliability, Process Control, Process Deviation, IPC J-STD-001G, Amendment 1 Cleanliness

INTRODUCTION

Highly dense electronic assemblies incorporate bottom terminated components. Miniaturized components create numerous challenges resulting in a shorter distance between conductors of opposite polarity, solder sphere size reduction, low standoff gaps, flux entrapment under the bottom termination, blocked outgassing channels, and more significant potential for leakage currents.[1]

In the presence of humidity, moisture (mono-layers of water) hydrogen bonds with ionic contaminants to create an electrolytic solution. Ions such as flux activators can dissolve metal oxides present in the flux residue at the soldered connection.[2] When the system is in operation, the electrical field attraction of the positively charged metal ions will migrate to the negative conductor. These metal ions can plate small dendrites, which result in leakage currents and/or parasitic leakage. As such, ionic residue testing is used to test for problematic residues that could hinder reliable circuit function.[3]

The core concept for materials compatibility and residue acceptability is a qualified manufacturing process (QMP).[4] In a QMP, the manufacturing materials and processes used to produce electronic hardware have been benchmarked and validated against electrical performance in hot/humid conditions. The art of characterizing what chemical residues exist on a manufactured assembly allows an assembler to determine the impact of those residues on electrical performance. The test methodology is useful in developing a risk profile.

After a manufacturing process has been qualified, the next step is to define how that qualified manufacturing process will be monitored for ionic residues. The establishment of an ionic process monitoring plan is a requirement for mission-critical – high-reliability electronic products. The sampling plan for ionic residues should be periodic, and with sample sizes such that a manufacturer has confidence, the process is in control.

HIGH-PERFORMANCE ELECTRONIC PRODUCTS

The classification we build products to is IPC Class 3/A. The class 3/A boards call for very stringent manufacturing criteria since the boards must remain operational in critical conditions. The electronics must provide continued performance and performance on demand. When deployed, there can be no equipment

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downtime. The products must work every single time. They must work correctly!

Processes for building the electronics must be qualified and validated. No process residues are accepted. Once validated, there must be a process control plan. Site-specific characterization on components with the highest probability of electrochemical failures is required to ensure every component is reliable.

Materials characterization must be in compliance with IPC J-STD-001 [Rev. F – H] Amendment 1, cleanliness. Testing requires custom test boards that detect electrochemical reliability across different component designs. Once qualified, there must be a process control plan to monitor for cleanliness on challenging components and processes that are representative of production hardware.

PROBLEM STATEMENT

Highly dense electronics are now being designed with miniature components. Designs require leadless and bottom terminated components. These component types create numerous challenges. The problem is that these components trap flux residues under the bottom terminations. They are harder to clean. With a tighter pitch, there is a shorter distance between conductors of opposite polarity. Tighter pitch poses a greater risk to reliability.

Figure 1 is a QFN-88 component that had partially cleaned flux residues left under the bottom termination after cleaning. Surface Insulation testing detected leakage currents. The components were sheared off the board and inspected. Monitoring for these types of defects on high risk components offers a useful process control method.

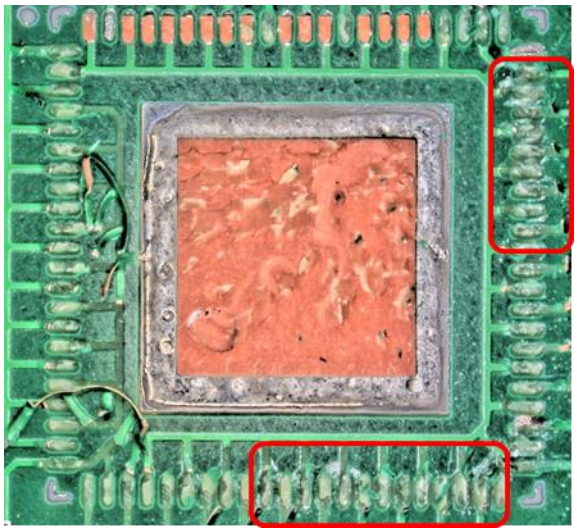

Figure 1: *QFN-88 that failed SIR testing*

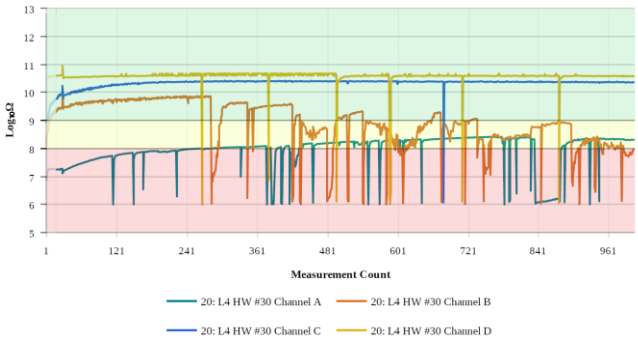

Figure 2: *Failed SIR Testing Result*

PROCESS CONTROL PLAN

Temperature-Humidity-Bias (SIR test method) was studied for use in developing a process control plan. Our operations favor electrical resistance measurement methods. The reason – electrical resistance measurement allow for the detection of process residues that are both ionic and non-ionic. These process residues are located under the components termination and commonly bridges conductor pathways. The residue is not visible to existing process control methods – specifically the resistance of solvent extraction (ROSE). We are looking for process deviations. Is our process consistent lot to lot – Is there variability?

IPC pass / fail for SIR testing is 8 $Log_{10}\Omega$s. For this experiment, we decided to build in a margin of safety by setting the lower SIR limit at 8.5 $Log_{10}\Omega$ resistance.

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Figure 3 illustrates the mean insulation resistance on a specific component. The lower and upper limit was set from 8.5 $Log_{10}\Omega s$ to 12.0 Log10Ωs. The chart shows that all ten boards tested were within the specification range.

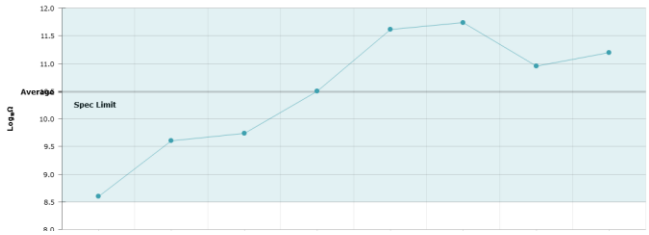

Figure 3: *Electrical Resistance of 8.5 – 12 $Log_{10}\Omega s$*

RESEARCH HYPOTHESES

Temperature / Humidity / Bias Hypotheses

1. Electrical resistance measurements under bias and elevated environmental conditions are long-accepted quality metrics
2. The first hours of a test card subjected to temperature/humidity/bias voltage represent the most ionic activity/change
3. This change can be used to determine the similarity of the process (similarly cleaned and produced boards should have similar starting resistance values, end resistance values, and general curve shape)
4. Deviation in process should be visible as a change

TEST BOARD

The QFN-88 and QFN-124 components were selected for this study. A custom SIR test board was designed with the QFNs horizontally positioned in Q1 & Q2. The QFNs were rotated 45° in Q3 & Q4.

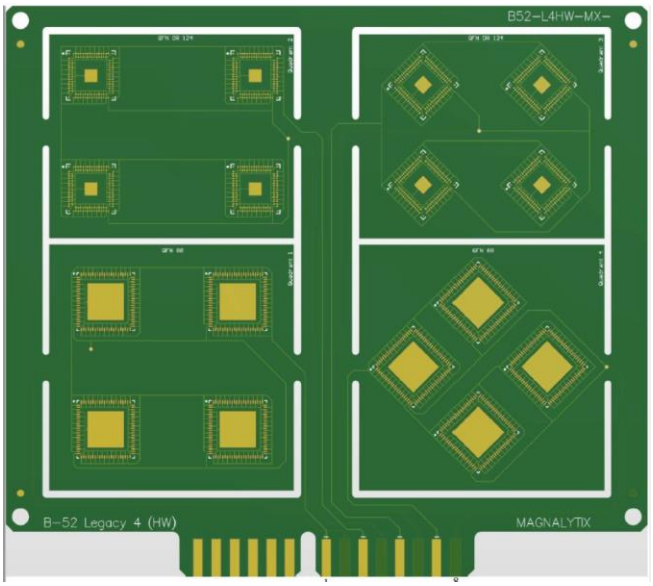

Figure 4: *SIR Test Vehicle*

QFN-88 Single Row Component

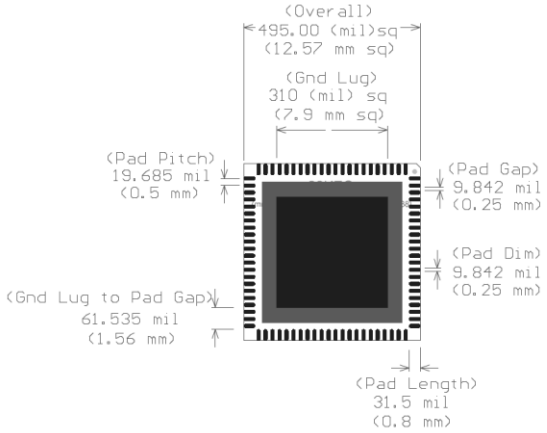

Figure 5*: QFN-88 dimensions*

The QFN 88 CHIP - 0.5 mm pitch is representative of production hardware. The tight pitch and large thermal lug are useful in defining cleanliness levels under similar component package styles. This part can be used to test no clean flux systems for SIR cleanliness levels as well as to determine if the cleaning process is capable and efficient in achieving the desired SIR levels for these types of component packages.

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QFN-124 Dual Row Component

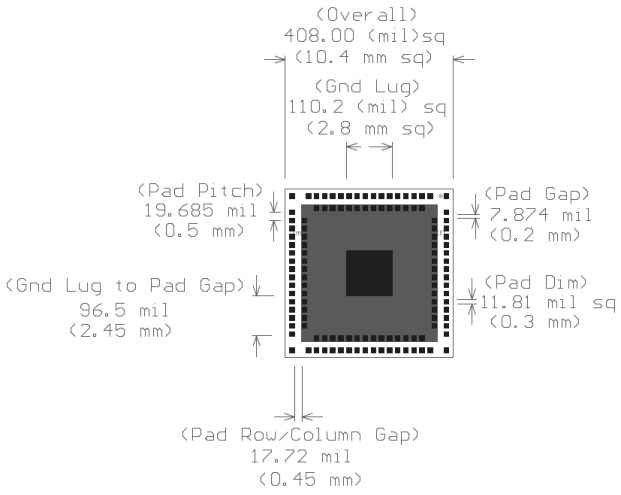

Figure 6: *QFN-124 dimensions*

The QFN-124 CHIP has a 0.5 mm pitch Bottom Terminated Component. This QFN-124 has a dual row pin out with ground lug, which makes this particular BTC more challenging than the Standard QFN Package style, which is a single row around the periphery of the package.

EXPERIMENTAL

PHASE 1: Data collection

- Perform a series of temperature-humidity-bias tests with the same card, to monitor process deviations
- Perform ROSE as a direct comparison
- Collect the raw data and analyze the data for statistical significance within several blocks of time (first 30 min, first hour, 2 hours, 6 hours, etc.)

PHASE 2: Process Deviation Monitoring

- Tests must all be run under the same conditions
  - Ramp speed of the chamber will be a factor, so it will be critical to make sure all tests are run with the same chamber
  - Chamber control feature should be used on a powered down the chamber to ensure that all tests start under the same ambient conditions and rise in a similar fashion
- Tests must all be ended at the same time
  - For this experiment, analyze the data within defined periods.

The SIR testing unit Process Control module allows the user to "Create & Manage their Test Boards." There are specific fields that will enable one to set up a particular process control profile. For each channel on the test board, the user can name the profile, and set an upper and lower specification limit. Other settings include time duration, measurement interval, temperature, relative humidity, bias voltage, and measurement voltage.

DATA FINDINGS

Twenty test boards were assembled and cleaned using defined process settings. The test boards were subjected to SIR testing using the following settings.

- Temperature: 40°C
- Relative Humidity: 90%
- Bias Voltage: 5 Volts
- Measurement Voltage: 5 Volts
- Measurement Interval: 5 minutes

The results were analyzed over a variety of periods. Baseline ROSE testing was performed on test samples.

Figure 7 is a chart of the SIR results for Board #11. Channels A&D represented the QFN-88, and Channels B&C represented the QFN-124. The QFN-88 values were below the lower limit, which is not acceptable. The QFN-124 values were acceptable.

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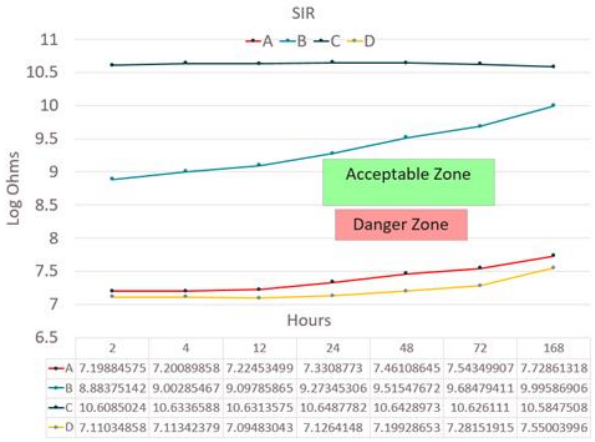
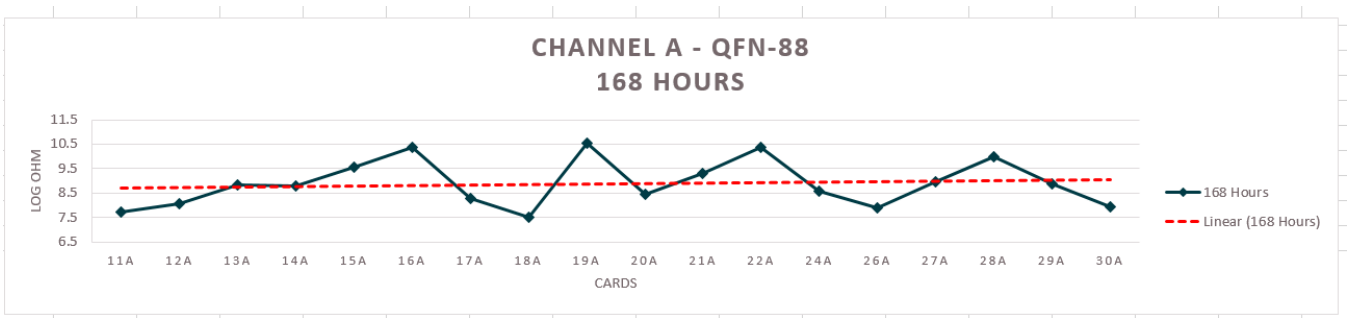


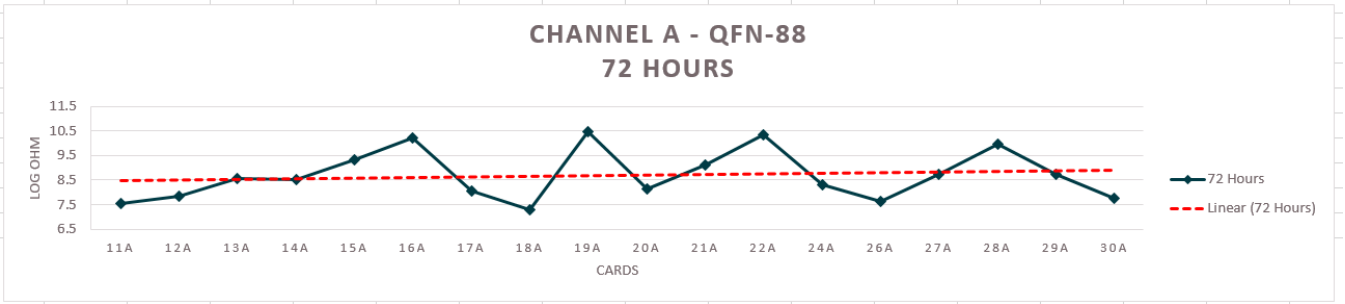
	2	4	12	24	48	72	168
A	7.19884575	7.20089858	7.22453499	7.3308773	7.46108645	7.54349907	7.72861318
B	8.88375142	9.00285467	9.09785865	9.27345306	9.51547672	9.68479411	9.99586906
C	10.6085024	10.6336588	10.6313575	10.6487782	10.6428973	10.626111	10.5847508
D	7.11034858	7.11342379	7.09483043	7.1264148	7.19928653	7.28151915	7.55003996

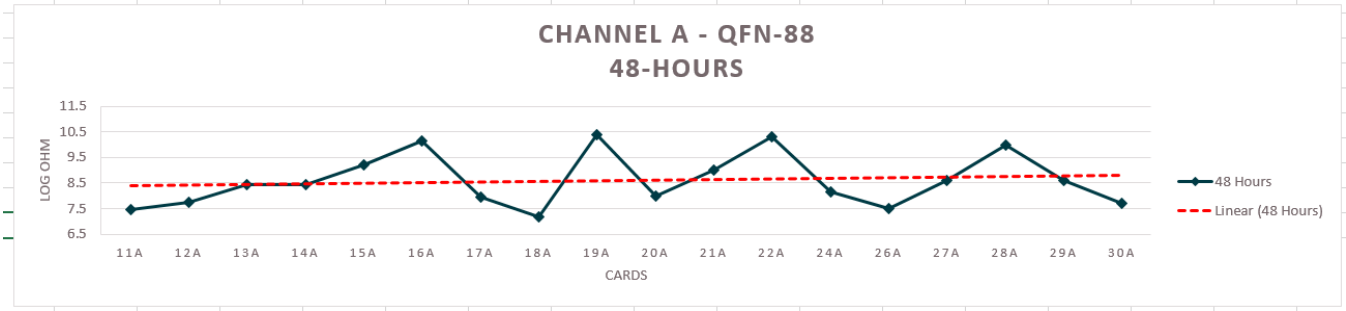
***Figure 7**: SIR test values for Board #11*

In a review of the data, we noticed parallels between the early-stage data and the full 168-hour data that supported our hypothesis. Now, let's have a look at the Mean data for each of the 4-channels on all 20 test cards in our data set.

QFN-88 Channel A







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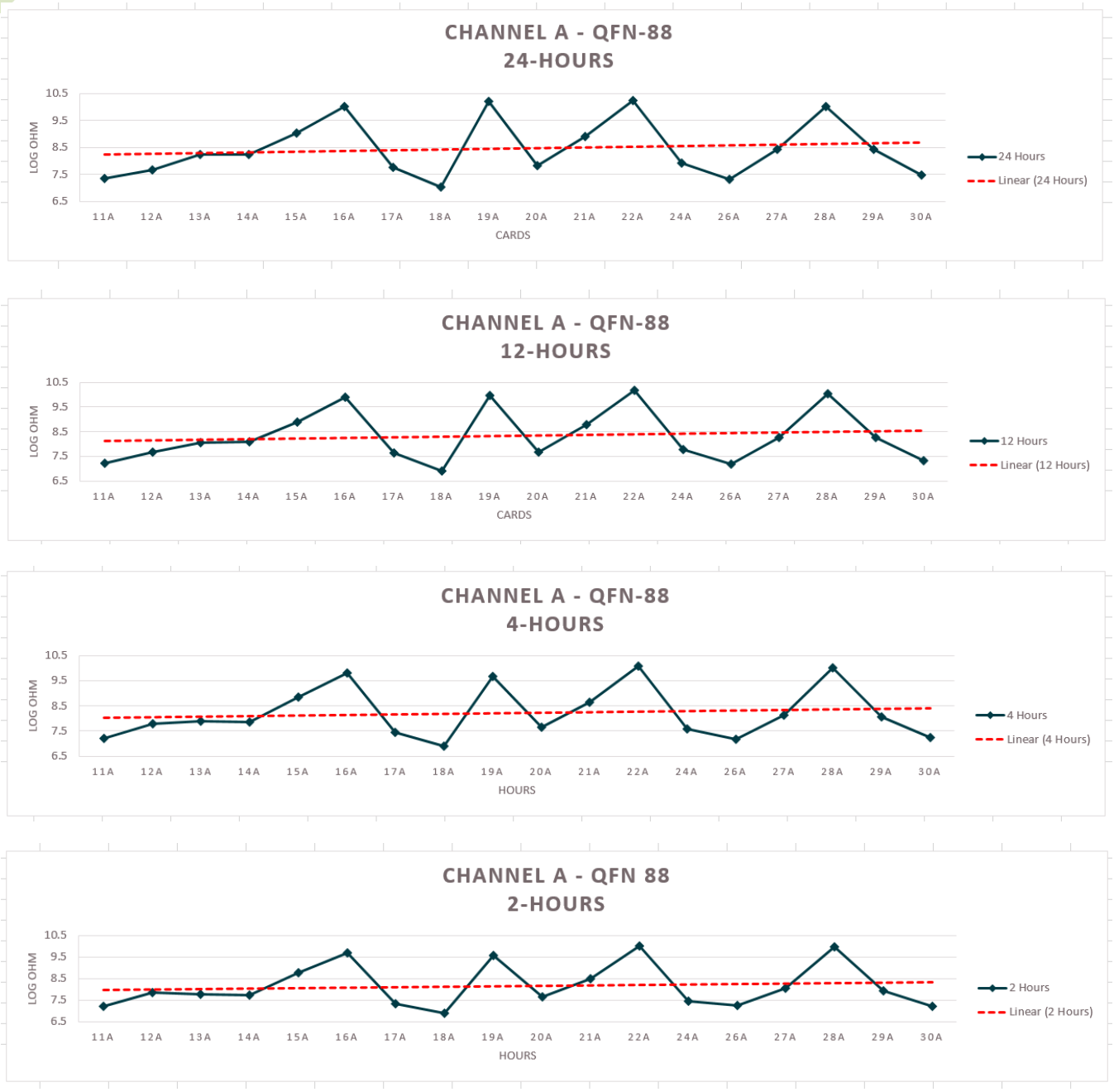

Figure 8: *Channel A Charts Plotted over Different Time Periods*

QFN-124 Channel B

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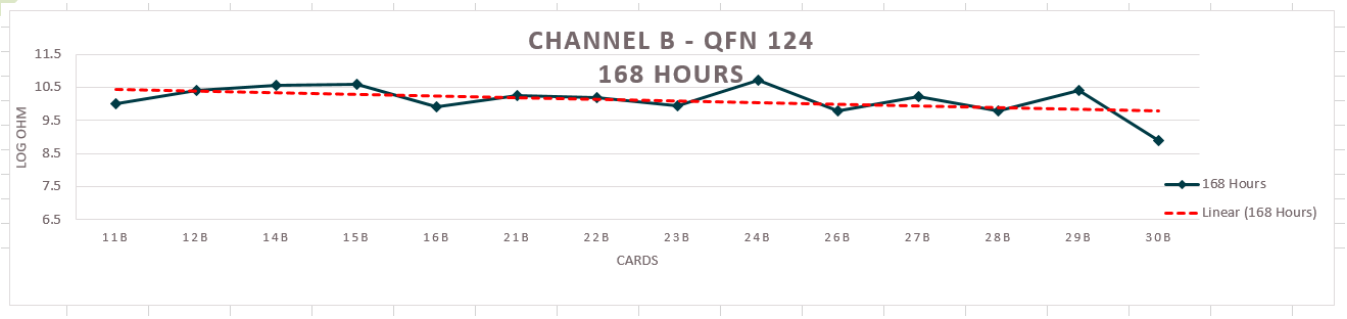

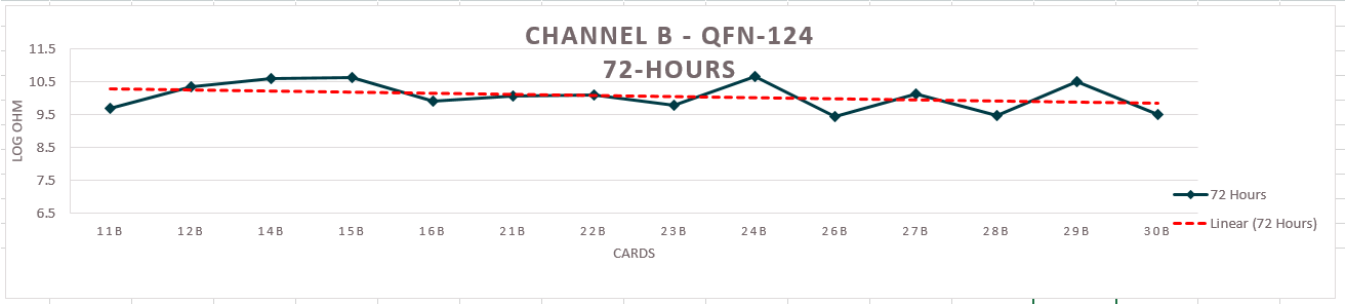

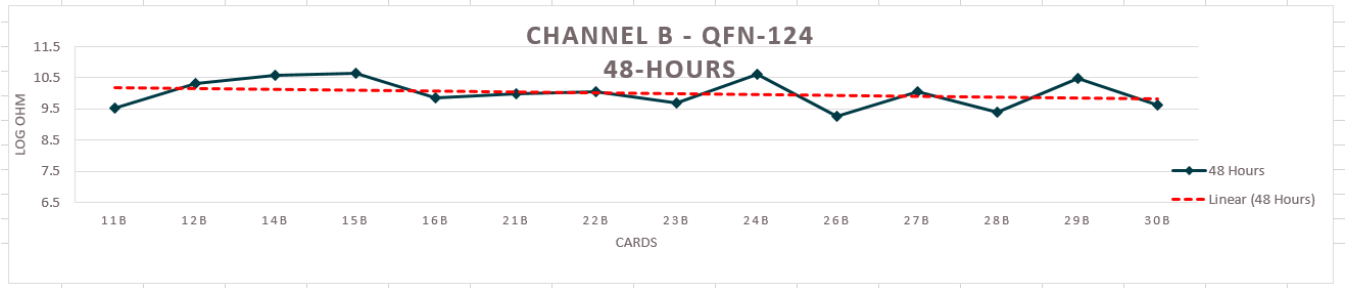

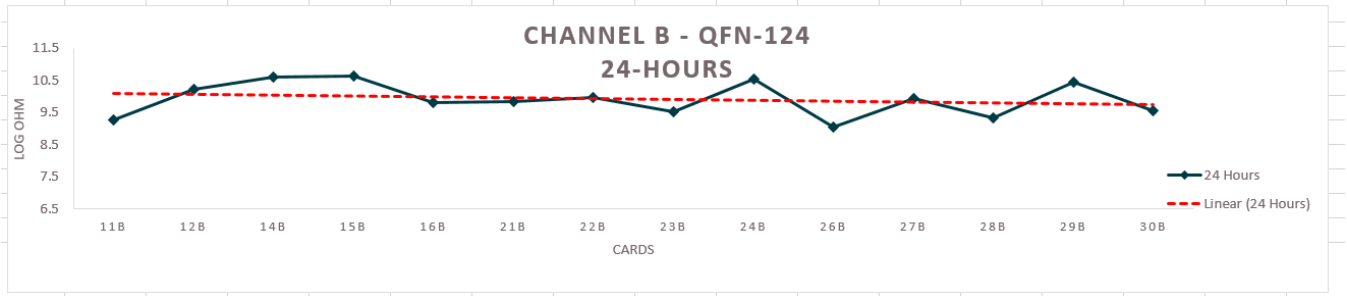

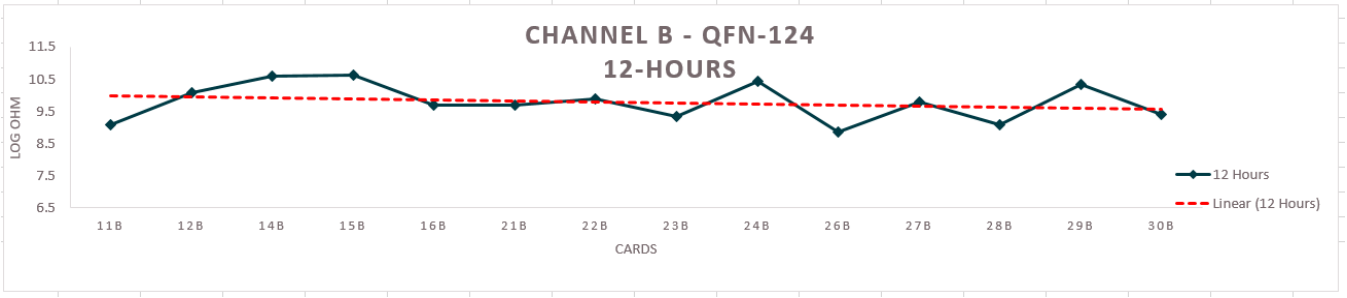

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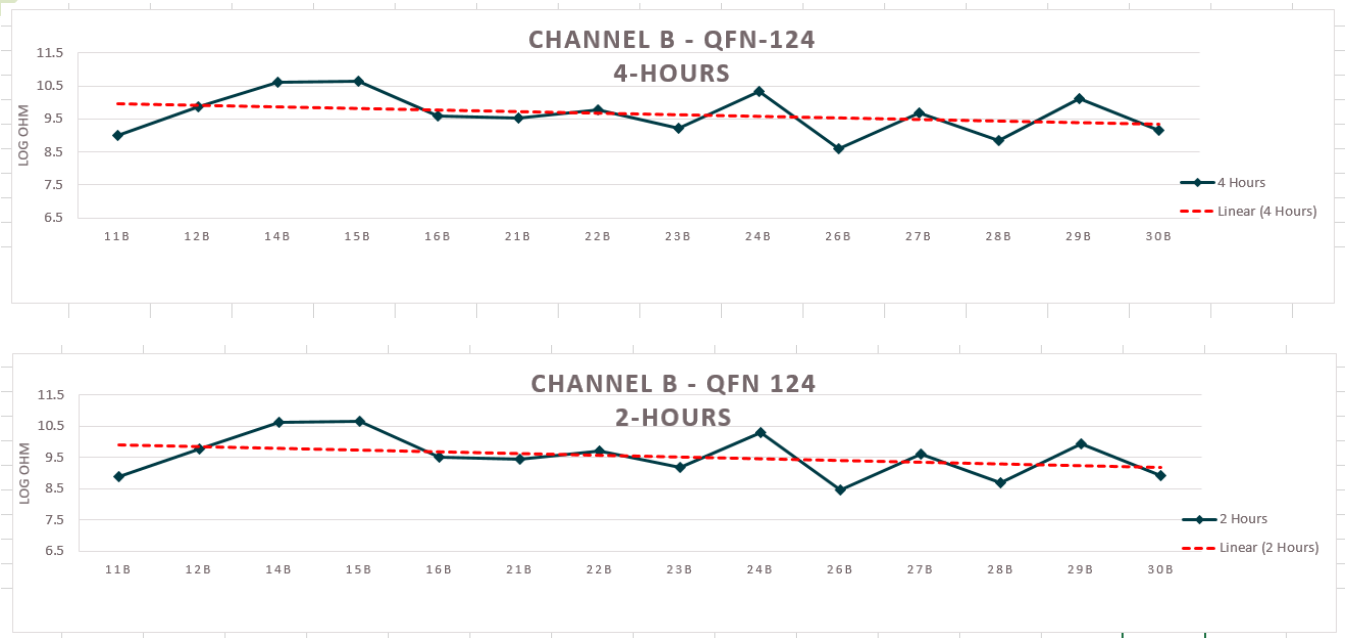
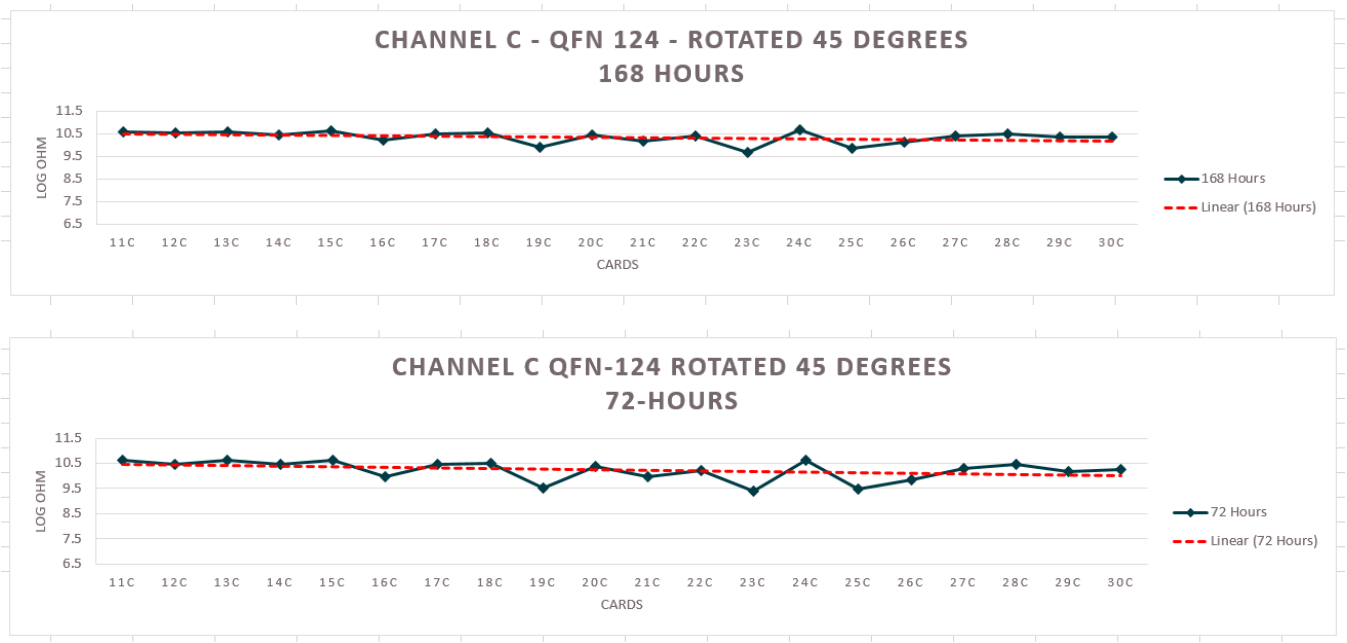


Figure 9: *Channel B Charts Plotted over Different Time Periods*

QFN-124 Channel C

Rotated 45°



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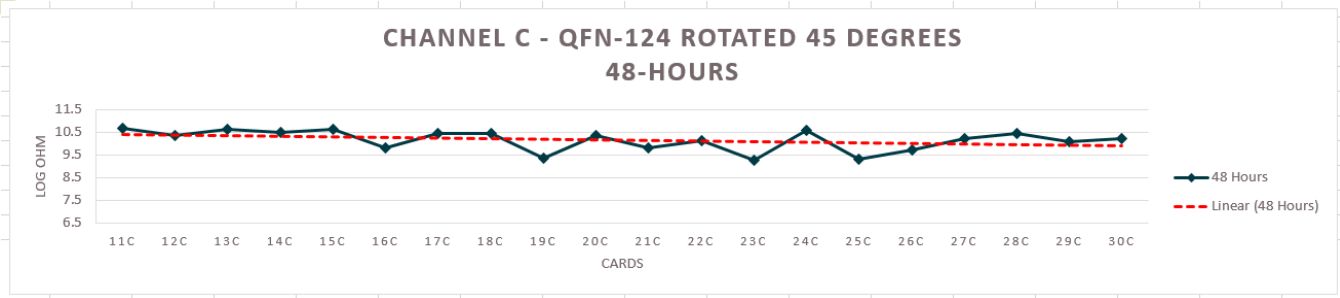

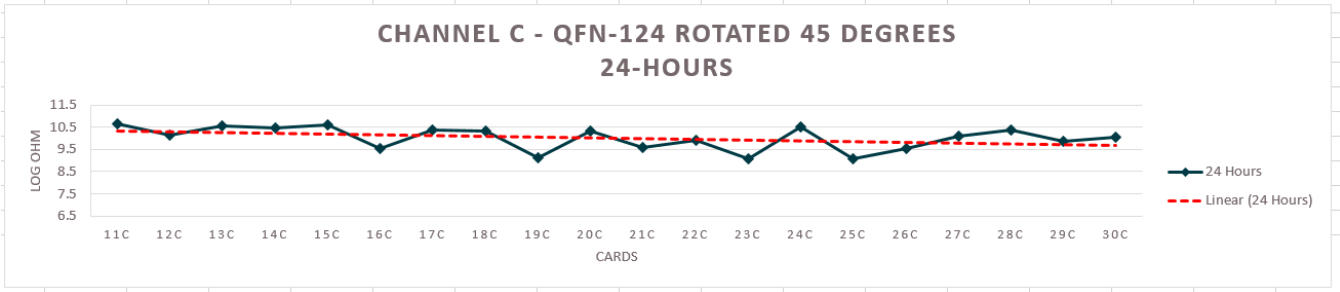

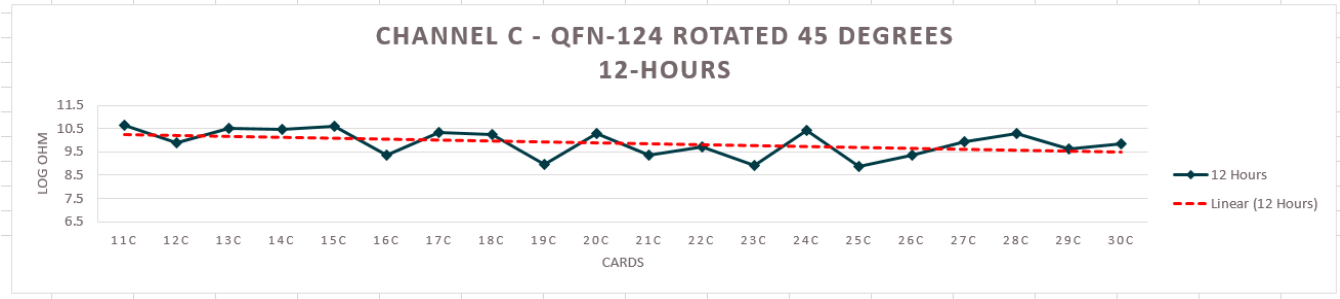

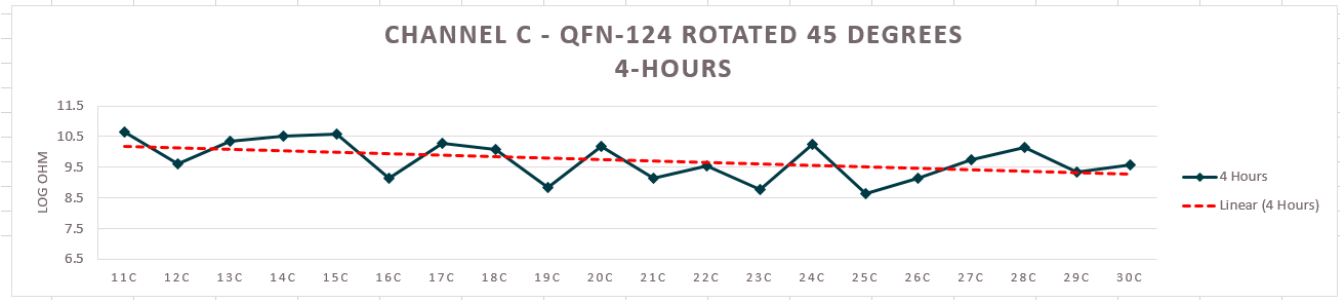

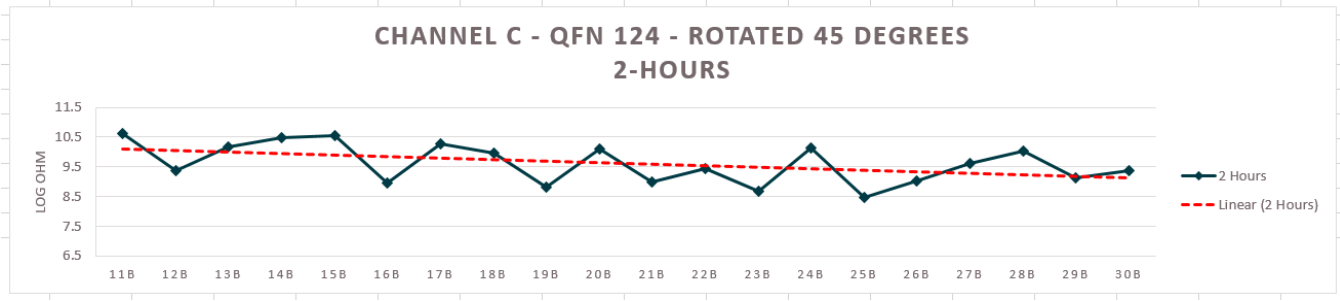

Figure 10: *Channel C Charts Plotted over Different Time Periods*

QFN-88 Channel D

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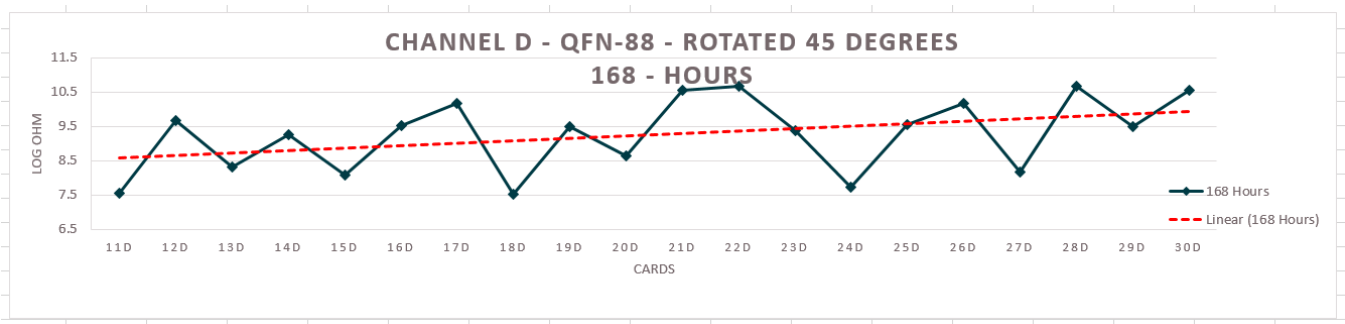
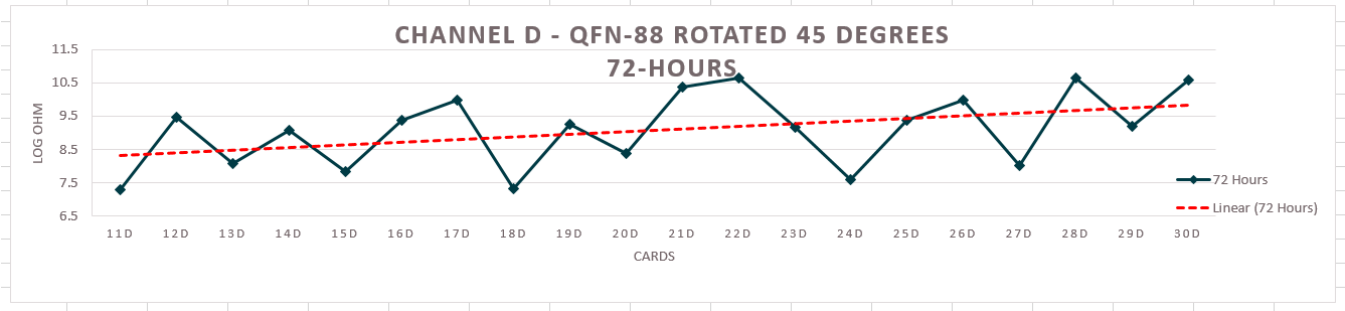
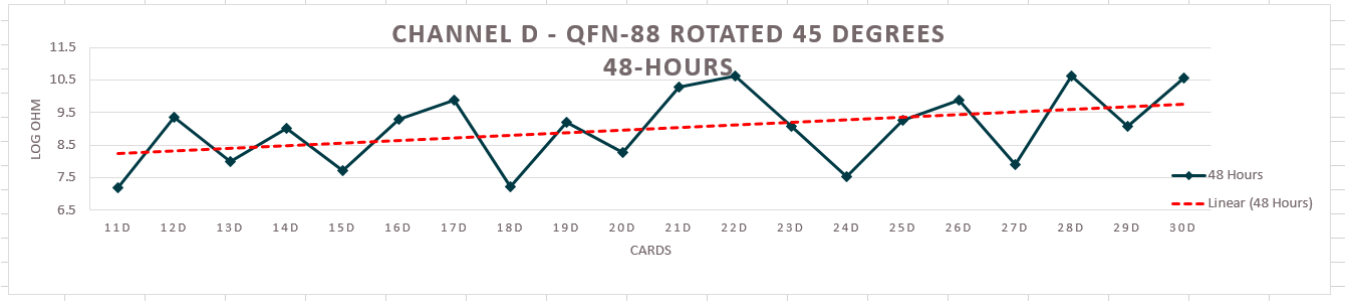
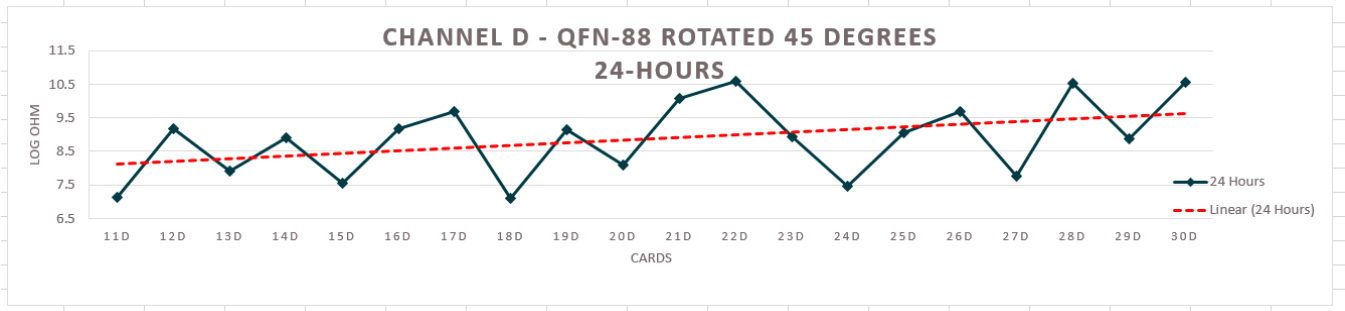
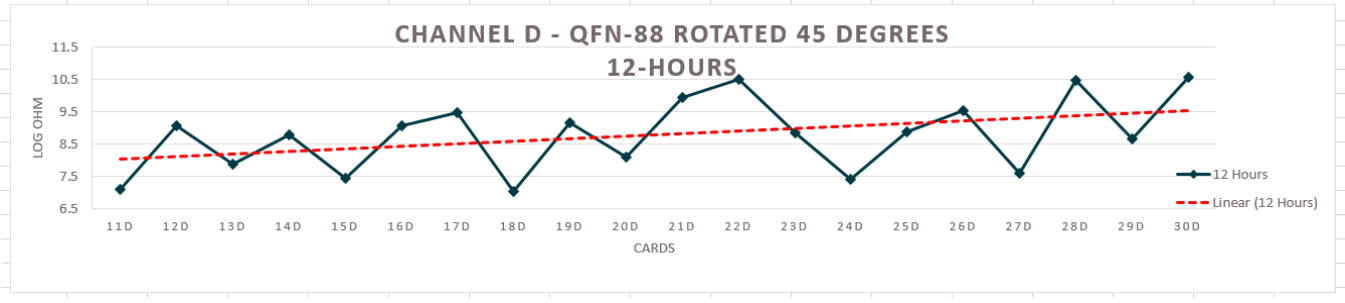
Rotated 45°











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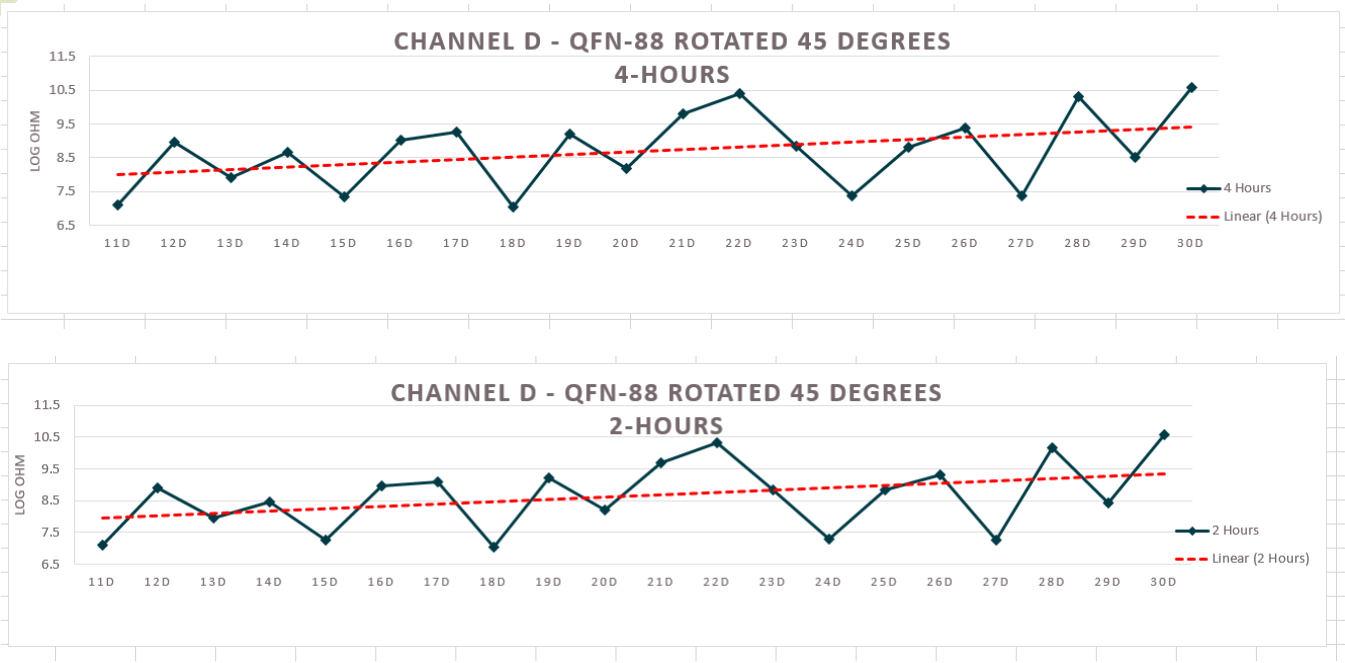

Figure 11: *Channel D Charts Plotted over Different Time Periods*

Following the SIR testing, each of the 20-boards was ROSE tested.

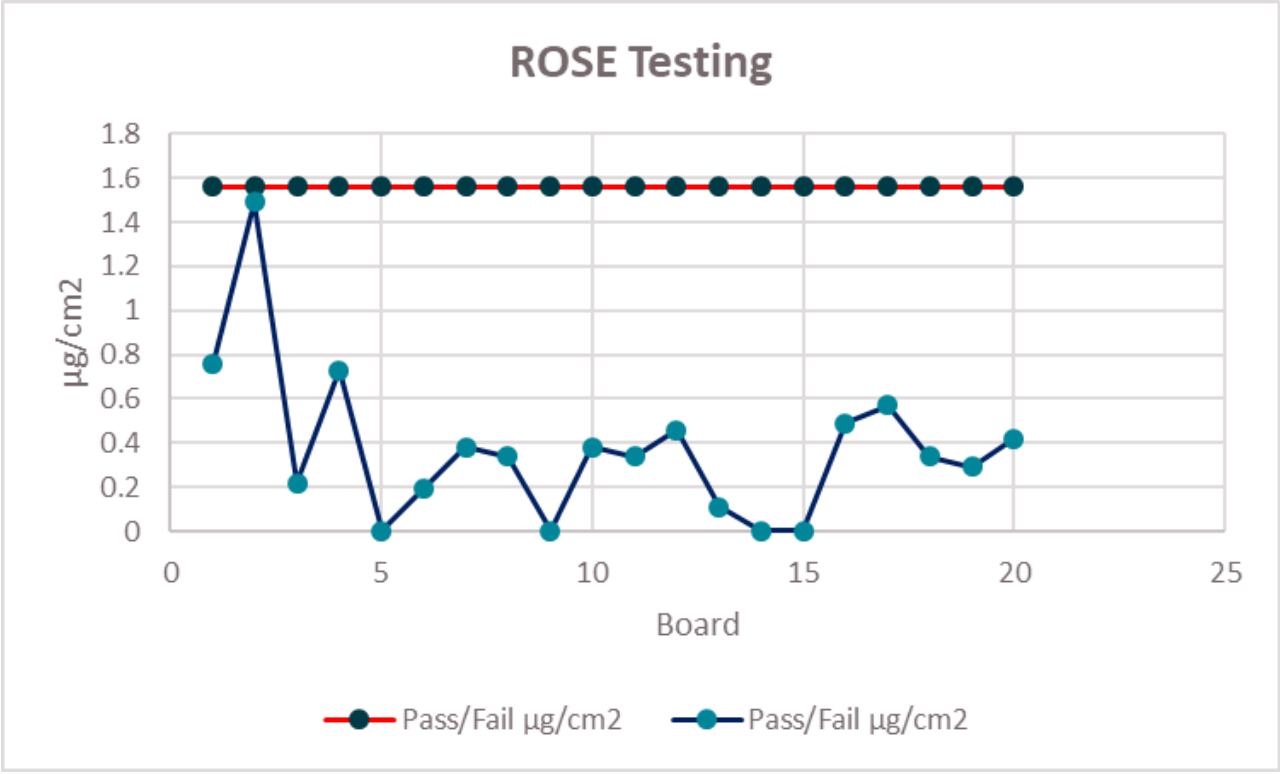

Figure 12: *ROSE Testing for Each Board*

DATA ANALYSIS

- Data was initially plotted in its entirety to look at overall trends
- A smoothing function was applied to visualize the

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trend in the data better.

- General observations:
  - Dual row QFN-124 had a SIR profile that appears to be more promising due to a tighter standard deviation
  - QFN-88 had a relatively uniform spread of data over the range of 7 to 11 $Log_{10}\Omega$s. Many data points were below the lower limits. Clearly, the cleaning process was not properly dialed in to clean this part within the Upper and Lower specification limits.
  - The higher variation QFN-88 results in a higher standard deviation. A higher standard deviation indicates a lack of consistency in regards to ionic residue present at the signal pins and under the component termination.

Figures 13 and 14 represents the average SIR values per hour of testing.

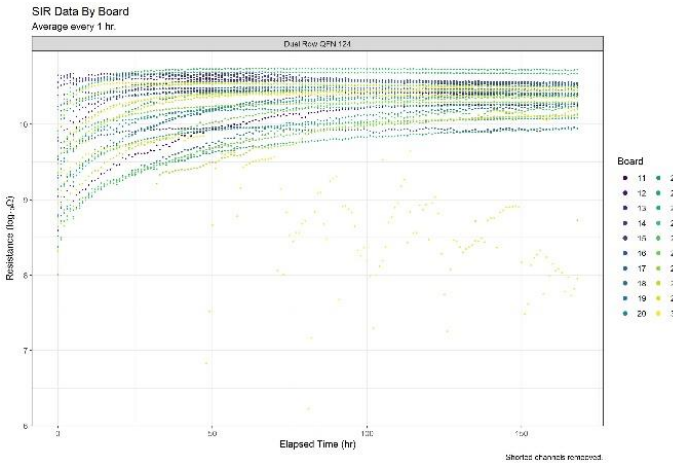

Figure 13: *QFN-124 Average per Hour*

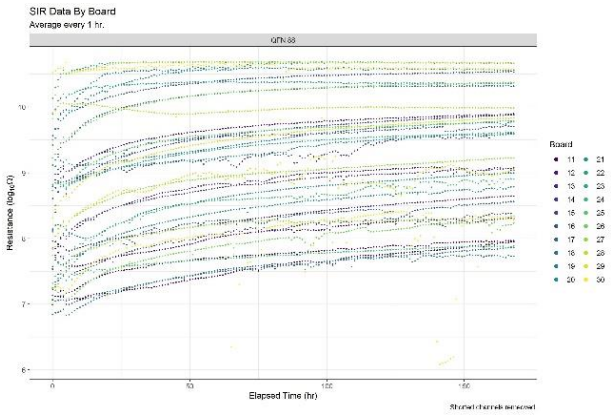

Figure 14: *QFN-88 Average per Hour*

The mean and standard deviation were plotted over time

- SIR value tends to start to flatten out around 50 hours
- Specific periods had larger variation than others
- Probably noise-related

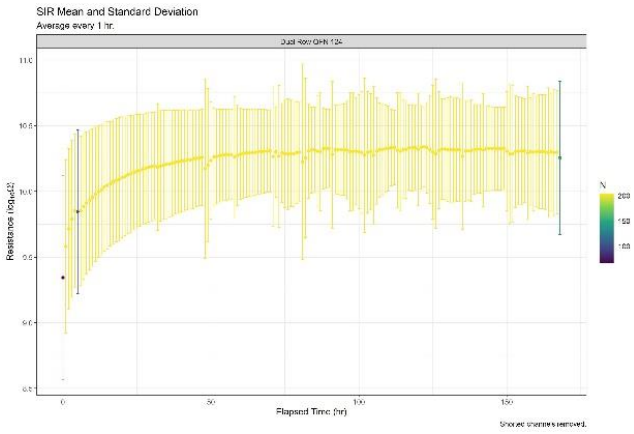

Figure 15: *QFN-124 Mean and Standard Deviation Averaged Every Hour*

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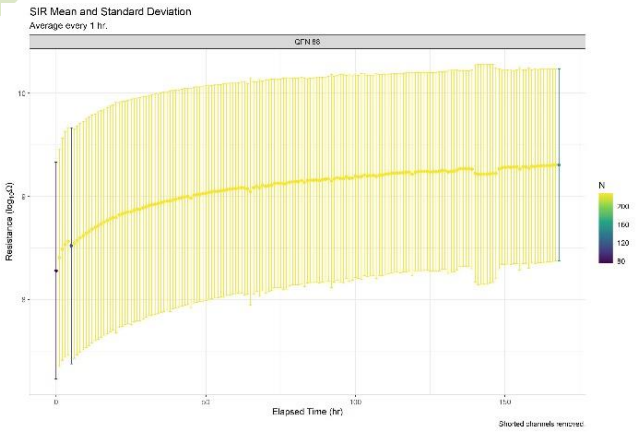

Figure 16: *QFN-88 Mean and Standard Deviation Averaged Every Hour*

INFERENCES FROM THE DATA FINDINGS

Electrochemical risk factors are not consistent across a printed circuit board; instead, they are specific to components that trap residues under the bottom termination and next to signal pins. The data finds different meaningful results between the QFN-88 and QFN-124.

In this study,

- QFN-88 was harder to clean
- There wash higher variability
- QFN-88 had many unacceptable results

Temperature-Humidity-Bias Environment

- Induces defects from ionic residues on targeted components
- Induces defects from non-ionic residues on target components
- These defects are reflective of undesirable process deviations
- Electrochemical risk is by nature site-specific rather than an average risk assessment

Inferences include:

- The large standard deviations on the QFN-88 component requires more work in optimizing the cleaning process.
- Temperature-humidity-bias testing is useful in determining the similarity of the process.
- A shorter SIR test time can detect process deviations.
- Contamination is not consistent across of the printed circuit board.
- Some component types are at a greater risk of electrochemical failure.
- ROSE testing is not a predictable method for site-specific testing.

RESEARCH HYPOTHESES

Hypothesis #1: Electrical resistance measurements under bias and elevated environmental conditions are long-accepted quality metrics

Hypothesis # 1 is accepted for the following reasons:

SIR testing is considered the gold standard for detecting ionic contamination. SIR is the best test method for determining the electrochemical reliability of:

- High-density interconnected board designs populated with miniaturized leadless and bottom terminated components.
- Multiple soldering operations that include SMT components on the top and bottom side of the board
- Thru-hole processes using both wave and selective soldering
- Rework and repair operations
- Conformal coating materials characterization

Hypothesis #2: The first hours of a test card subjected to temperature/humidity/bias voltage represent the most ionic activity/change

Hypothesis #2 is accepted/ rejected for the following reasons:

Accepted: When ionic contamination is present, surface insulation resistance will be lower at the

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beginning of the test. The QFN-88 insulation resistance had lower insulation resistance at the beginning of the test. As the test ran, the insulation resistance improved due to the ionic residue drying out and not being mobile in mono-layers of water present in the humid environment.

Rejected: A short test period does not detect leakage currents and dendritic formations. These typically require longer test time to form and propagate.

Hypothesis #3: This change can be used to determine the similarity of the process (similarly, cleaned and produced boards should have similar starting resistance values, end resistance values, and general curve shape).

Hypothesis #3 is accepted for the following reason:

The research finds that much can be learned from careful analysis of the first hours of the long accepted SIR test method. The first hours clearly detect process contamination that reduces insulation resistance.

Hypothesis #4: Deviation in process should be visible as a change

Hypothesis #4 is accepted for the following reason:

The QFN-88 was clearly different from the QFN-124. Process contamination was detected.

CONCLUSION

Electrical testing results, with power on, during extremes of temperature and humidity, detects the presence of ionic contamination. The challenge industry faces today is that the risk factor for electrochemical failures is not the same across a printed circuit board. The risk is site-specific, being more problematic across different components.

Process Control requires an objective sampling plan for measuring ionic residues of the process. This study looked at two test methods. The ROSE bulk extraction test method is a non-destructive test method that can be used on the actual product. The problem is that this method is not consistent in detecting problematic residues across site-specific components.

Electrical testing using SIR temperature-humidity-bias is far superior test method. The problem with this method is that it cannot be used on the actual production board. This method requires a test board or coupon that is representative of the complex components used on production hardware. When using a representative test board or coupon, this test method can be used to monitor and control the process with accuracy.

FOLLOW-ON RESEARCH

Follow-on research is needed to develop a “Process Control Plan.”

The research team plans to perform a series of tests by first developing the “golden image” to define upper and lower process limits.

Using the same test card, the process will be varied to validate the method work for detecting the cleanliness state.

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